PRECISION THERMOMETRIC SYSTEM USING RADIO TELEMETRY WITH COMPUTER INTERFACING

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CERTIFICATION

We certify that this research work and the results obtained was carried out by Odo Ayodele of the department of Physics F.U.T. Akure and had been approved as meeting the requirement for the award of M.Tech. Degree in Physics of the Federal University of Technology Akure, Ondo state Nigeria

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DEDICATION

This work is dedicated to my mother Bola Odo-Alawaye

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ABSTRACT.

A precise temperature monitoring system in the range 50—1350°C using Radio Telemetry as a means of signal transmission has been designed and constructed.

It consists of a sensitive thermocouple amplifier with active cold junction compensation. To enable FM Telemetry, the output voltage was linearly converted into pulses of proportional frequency and then pulse modulated for transmission as radio signals. The signal is then demodulated by a VHF receiver and subsequently processed. The system, which consists of two modules works as a general-purpose temperature-monitoring device with an accuracy of ± 1°C. For the purpose of data logging the measured temperature, a precise computer-interfacing adapter was also designed and constructed. It includes a TC7109 12-bit A/D converter and two octal D-type latches which provide the handshaking and necessary multiplexing action required to input 12-bit through the 8-bit data port available for input on the parallel port of the computer. The unit is designed to enable its use as a general-purpose device for other inputs other than a thermocouple amplifier output. The software for the control, data processing and presentation of output (result of computation) on a graphical screen of the VDU of the computer was written in QBasic and Visual Basic, the codes of which can easily be adapted to suit the user's purpose.

CHAPTER ONE

INTRODUCTION

1.1 OVERVIEW

Temperature measurement and control have become a very important process in many industrial and scientific researches. Isaac et al. (1993) have described the development of a precise temperature measurement circuit to meet various required standards of operation. It is however a common knowledge that such circuits, especially those meant for high temperatures suffer from low accuracy and stability. The basic reason being that such circuits utilise thermocouples as input devices, whose low sensitivity, high susceptibility to noise pick-up and need for cold junction compensation impose many limitations.

In many scientific applications such as in the heat treatment of materials in an electric oven, reproducibility of materials of some desired quality and properties is often the goal. Material properties are known to depend largely on the heat treatment temperature and for how long the temperature is fixed at the desired tempering value (Kawser, 1993). It becomes necessary therefore to focus much more on the temperature control device for such an oven, which in most cases starts with the thermocouple amplifier. How precise this amplifier tracks the temperature in the furnace definitely affects the overall controllability of such a furnace.

In yet other applications, in which interconnecting wires between the thermocouple and the visual output device are not feasible, such as in the case in which the system has moving components (e.g. the rotary furnace), it becomes necessary to device another means of signal transmission different from the traditional thermocouple-wire through panel meter. The use of split rings has been reported, but it falls short from contact resistance developed at the junction of the slider (Marrangoni, 1993).

The use of radio telemetry has been well established as a preferred means of signal transmission where accessibility is a major problem. It has been the technique of choice for the tracking and collation of data from biological specimens, for data communication via satellites and for the control of robots located in remote areas (Young, 2001).

The advancement attained in modern computer architecture in the area of speed of processing, and the capacity to store large amounts of data, coupled with the ease and flexibility of present programming languages, has resulted either in dedicated or general purpose personal or small computers. And today it has become a natural adjunct to a measurement system. Computers may be used simply to monitor and record one or more measurements or they may serve as an interactive part of a more comprehensive measurement and control system (Marrangoni, 1993).

Researchers in the field of measurement and instrumentation are still finding new and improved ways of adapting the computer as a research tool for experimental purposes. To connect common measurement circuitry to a computer requires considerably more understanding of the functioning of systems than it would first appear to be. The output from most transducers applied for measurement purposes originate as analogue type signals (Usher, 1989), but the computer recognises only digital quantities. As a result, often the first requirement is to change the data form by means of an analogue-to-digital converter. In addition, data from circuitry external to the computer must be fed to the computer in a form and order that the computer is prepared to accept.

The modern computer connection to the outside world through its ports is generally bi-directional. Computers receive or output data in a well defined and orderly manner, as prescribed by the controlling software, i.e. a programme written to control the activities and interaction of the computer main hardware with external circuitry. In addition input/output data may be handled in either serial or parallel form (Stewart, 2001).

1.2 OBJECTIVE AND SCOPE

It is the aim of this project to:

1. Present a thermocouple amplifier of high precision with an active cold junction compensation capable of amplifying a thermocouple output signal over the temperature range 50 – 1500°C, with little drift with time and variation in ambient temperature.
2. Device a means of faithfully transmitting the output signal from the thermocouple amplifier through radio telemetry to a VHF receiver, located 20 meters away from the measuring zone.
3. Design and construct a 12-bit interfacing adapter for an IBM personal computer, using its printer's port as a channel for the control and transmission of data.
4. Develop a software for the control of the attached interfacing circuitry, data acquisition from the circuitry and further processing of the data. And finally displaying the result on the visual display unit of the computer, while at the same time storing the acquired data against time in a data file for subsequent analysis of temperature variation with time.

1.3 BASIC HARDWARE DESIGN AND SOFTWARE DESIGN FEATURES

Fig.1.1 shows the overall block diagram of how the entire process of temperature measurement using radio telemetry was achieved. The system starts with the thermocouple, with its hot junction placed in the area where the temperature is desired. The output from the thermocouple, which is a direct current (d.c.) voltage is fed into the thermocouple amplifier which provides the necessary thermocouple cold junction compensation and enough amplification to allow for further processing of the signal.

The output signal from the thermocouple amplifier is then converted into pulses by a linear voltage-to-frequency converter trimmed to give an output of 1Hz/mV. This output signal from the converter then pulse modulates an FM wave transmitted at a carrier frequency of 220MHz and then a VHF receiver is used to demodulate the transmitted signal at the receiving end. The demodulated signal, which appears as pulses of frequency equal to that transmitted, is then converted back to voltage by a linear frequency-to-voltage converter trimmed to produce an output of 1mV/Hz. The output, a d.c. voltage is signal conditioned to remove ripples, buffered by a unity gain amplifier and then fed to an analogue-to-digital converter.

Conversion of the analogue input signal to digital form starts with the 12-bit A/D converter. The converter is a 12-bit ADC IC (TC7109) from Microchip. From the microchip semiconductor data sheet, it is found that the device offers the following outstanding features, low noise, zero integrator cycle for fast recovery from input overloads, and no zero adjustment needed. This makes the device a good choice for continuous conversion. For direct interfacing, the combination of chip-enable and byte-enable control signal is necessary, this is provided by the software designed for such. Although the TC7109 IC incorporates the circuit necessary for direct interfacing and multiplexing of data, it is desired for increased efficiency to allow the A/D converter run continuously and present data without interruption. A separate circuit consisting of two D-type latches was therefore introduced to provide the needed multiplexing of data.

The D-type octal latches (74LS373) has an enable input (pin 11) which when set high allows the output to follow the A/D converter output and latches the output when set low. It also has an enable output (i.e. pin 1) which when set high sets the eight outputs to high impedance. It is this feature that was exploited in the software design.

The channel for data transmission into the computer is the printer's port which consists of three parallel ports; namely the control, data and status ports (Stewart, 2001). Since the A/D converter is set for continuous conversion operation the computer need not check its status. Therefore only the control and data ports of the printer were used.

A common limitation of the parallel port is that it can only take eight bits of data through its data port at a single time (Anderson, 1996). The software is therefore designed to control the interfacing circuit such that the 12-bit output from the A/D converter is presented as two bytes of data, read through the data port in succession of 8 bits and then 4 bits. The data received by the computer is then processed and displayed as true temperature reading on the visual display unit of the computer. The creation of files for both read and write operations is also handled by the software.

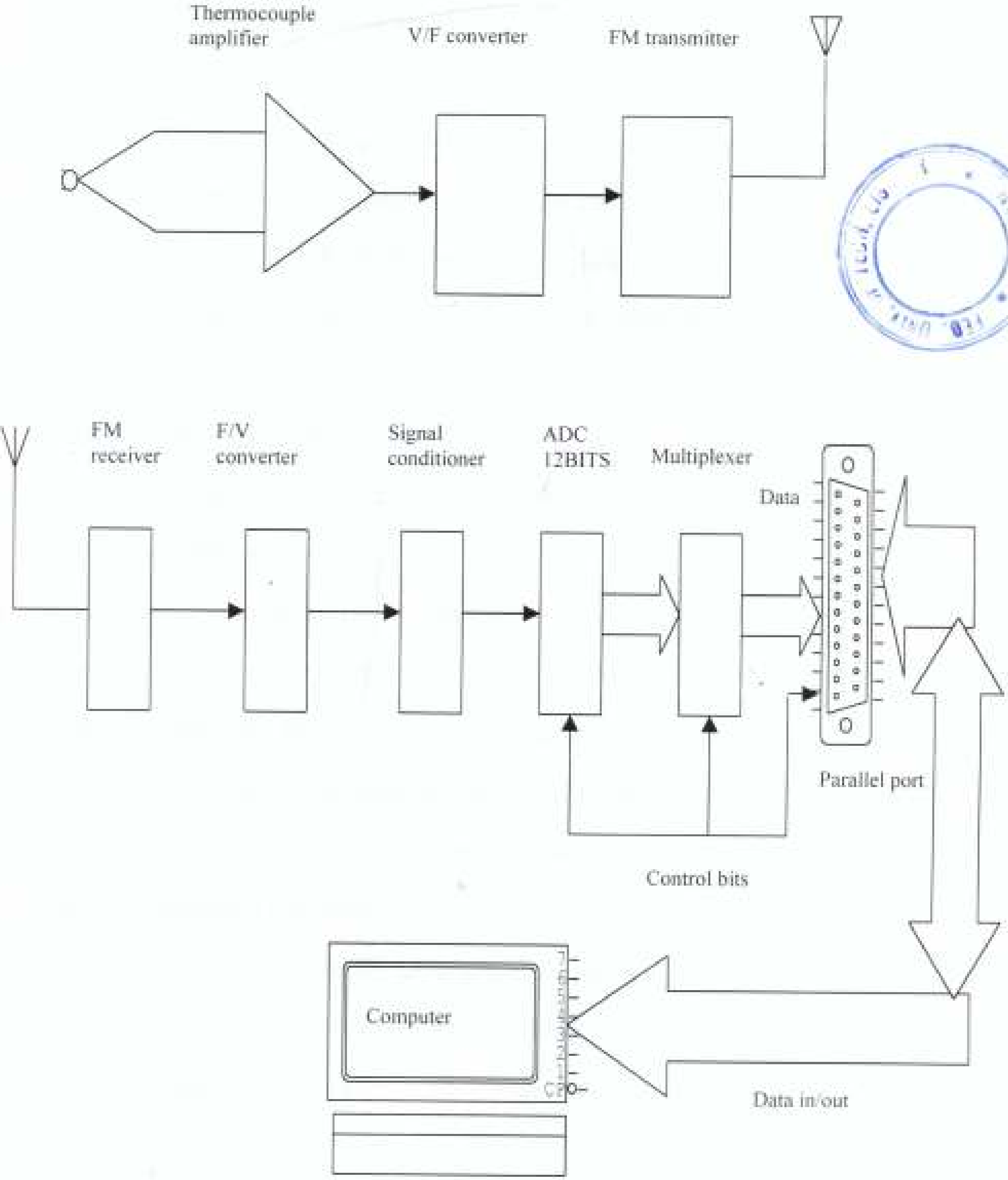


Fig 1.1: The block diagram of the thermometric system

CHAPTER TWO

LITERATURE REVIEW

2.1 TEMPERATURE STANDARD

The international measuring system sets up standards for only four fundamental quantities, length, time, mass, and temperature. Temperature is fundamentally different in nature from length, time and mass, in that it is an intensive quantity whereas the others are extensive. The idea of a standard unit of mass, length or time that can be divided or multiplied indefinitely to generate any arbitrary magnitude of these quantities cannot be carried over to the concept of temperature. The fundamental meaning of temperature, just as for all basic concepts of physics, is not given easily. For most purposes the Zeroth Law of thermodynamics gives a useful concept. The Zeroth Law states that when two bodies are each in thermal equilibrium with a third body, they are in thermal equilibrium with each other. Then by definition the bodies are all at the same temperature. Thus if a reproducible means of establishing a range of temperatures can be set up, unknown temperatures of other bodies may be compared with the standard by subjecting any type of thermometer successively to the standard and to the unknown temperature and allowing equilibrium to occur in each case. That is the thermometer is calibrated against the standard and afterwards may be used to read unknown temperatures (Marrangoni, 1993).

In choosing the means of defining the standard temperature scale any of the many physical properties of materials that vary reproducibly with temperature could be employed. To define a temperature scale numerically we must choose a reference temperature and state a rule for defining the difference between this reference and any other temperature. Temperature is measured for some reasons, such as computing the thermal expansivity, rate of heat-transfer, electrical conductivity, gas pressure e.t.c. The form of the equation employed to make such calculations depends on the standard used to define temperature. A temperature scale that gives a simple form of thermal expansion equation may give complex form to any other physical relations involving temperature. Since this difficulty is common to all *standards* based on the properties of a particular substance, a way of defining a temperature scale independent of any substance is desirable.

The thermodynamic temperature scale in Kelvin proposed by Lord Kelvin provides the theoretical base for a temperature scale independent of any material property. If also a number is selected to describe the temperature of a chosen fixed point, then the temperature scale is completely defined. At present the fixed point is taken as the triple point of water because this is the most reproducible state known. The number assigned to this point is 273.16K. The international practical temperature scale is set up to conform as closely as practicable to the thermodynamic scale. At the triple point of water, the two dynamic scales are in exact agreement by definition. Five other fixed points are used. These are

(a) the boiling point of liquid oxygen (-182.962^0C)

(b) the boiling point of water 100^0C

(c) the freezing point of zinc (419.58^0C)

(d) the freezing point of silver (961.93^0C) and

(e) the freezing point of gold (1064.43^0C)

The accuracy of temperature standards may be considered from two points of view. First, how closely can the international practical temperature scale be reproduced? Second, how closely does it agree with the thermodynamic absolute scale? The highest reproducibility of the international practical temperature scale occurs at the triple point of water. This can be realised to a precision of a few ten–thousandeth of a degree, given an accuracy of about 1 Part Per Million (PPM). Calibration of a given temperature-measuring device generally is accomplished by subjecting it to some established fixed-point environment. Examples of these are the melting and boiling points of standard substances such as water, gold etc, or by comparing its reading with those of some more accurate (secondary standard) temperature sensor which itself has been calibrated.

2. 2 TEMPERATURE MEASURING METHODS.

Over the years various measuring devices have been developed based on the variation of material properties with temperature. Three basic methods have so far been fully developed and adapted to the measurement of temperature. These are:

(1.) Thermal expansion method: which is based on the thermal expansivity of some materials? Among the thermometer developed on this basis are:

(a) Bimetallic Thermometer (b) The Liquid-in-Glass Thermometer and

(c) The Pressure Thermometer.

(2.) Radiation method: this is based on the physical phenomenon that a body emits electromagnetic radiation of varying wavelength depending on the temperature of the body. An ideal radiator obeys Planck's law, which states that

$$\omega_{\lambda} = \frac{c_1}{\lambda^5 (e^{c_2/(\lambda T)} - 1)}$$

Where ω_λ is hemispherical spectral radiation intensity W/cm^2.μm; C_1 = 37.4/3 W.μm^4/cm^2 ; C_2 = 14.388 μm.K; λ is wavelength of radiation in μm; and T is absolute temperature of blackbody measured in Kelvin (K).

The optical pyrometer is the most commonly adaptable instrument for radiation measurement.

(3.) Thermoelectric method; this is based on the characteristic exhibited by most materials. When two metallic wires of different material composition are combined to form a junction, a d.c. voltage develops across their loose terminals, which varies with the temperature at which the junction thus formed is placed. In this work which involves the measurement of temperature above 1000°C in a rotary furnace, emphasis will be laid on thermoelectric devices

2.2.1 THERMOCOUPLES

If two wires of different materials A and B are connected as shown in Fig. 2.1 with one junction at temperature T_1 and the other at temperature T_2 a d.c. emf is developed across the terminals. This phenomenon is known as Seebeck effect. The magnitude of the voltage E depends on the two materials used to form the thermocouple and the junction temperature T_1 and T_2. When using a thermocouple, we are trying to measure the temperature of a body in contact with the thermo-junction. These two temperatures are not exactly the same, if an electric current is allowed to flow through the thermo-junction, heat is generated or absorbed at the junctions and thus makes one of the junctions hotter and the other colder than the surrounding medium whose temperature is being measured. This heating and cooling process is related to the Peltier effect.

If the thermocouple's output emf is measured with a potentiometer no current flows and thus Peltier heating and cooling is not observed. When a millivoltmeter is used instead, current flows and heat is absorbed at the hot junction (requiring it to become cooler than the surrounding medium) while heat is liberated at the cold junction, making it hotter than its surrounding medium. These heating and cooling effects are proportional to the current and fortunately are negligible when the current is that produced by the thermocouple itself in a practical millivoltmeter circuit. These errors are even less when the thermocouple is connected (as is very common) to an instrumentation amplifier with high input impedance (1 to 1,000MΩ).

Another reversible heat-flow effect, the Thomson effect, influences the temperature of the conductor between the junctions rather than the junctions themselves. When current flows through a conductor having a temperature gradient (and thus a heat flow) along its length, heat is liberated at any point where the current flow is in the same direction as the heat flow, while heat is absorbed at any point where these flows are opposite. Since this effect also depends on current flow, it is not present if a potentiometer is used; even if a millivoltmeter is employed the effect of the heat flow on the conductor is completely negligible.

Finally, it should be noted that in any current carrying conductor, the I^2Rt heat is generated thereby raising the circuit temperature above its local surroundings. Again potentiometric and high-input-impedance voltage measurement gives negligible error. Errors in millivoltmeter circuit usually are negligible but can be estimated if the heat transfer conditions are known. The above physical effects can be analysed on a macroscopic scale by classical thermodynamics taking into account the irreversible energy conversion process and the Peltier and Thomson effects. The total emf produced is made up of a part due to the Peltier effect, which is localised at each junction and a (usually much smaller) part caused by Thomson effect which is divisible along each conductor between the junctions. The Peltier emf is assumed proportional to the junction temperature, while the Thomson effect is proportional to the difference between the squares of the junction temperatures. For the total voltage, the equation takes the form:

$$E = C_1(T_1 - T_2) + C_2(T^2{}_1 - T^2{}_2) \tag{2.1}$$

Where E is total voltage (μV), T_1, T_2 = Absolute junction temperatures, in Kelvin (K).

Unfortunately the assumptions leading to equation (2.1) are not exactly satisfied in practice, thus this equation cannot usually be used to predict accurately temperature from measured voltages. As a result temperature measurement by thermoelectric means is thus based entirely on empirical calibrations and the application of so called thermoelectric laws, which experience has shown to hold. These laws are adequate for analysing most practical thermocouple circuit.

The Laws of thermocouple behaviour may be stated as follows:

(1) The thermal emf of a thermocouple with junction at T_1 and T_2 is totally unaffected by temperature elsewhere in the circuit if the two metals used are each homogeneous as shown in Fig. 2.2.

(2) If a third homogeneous metal C is inserted into A or B as shown in Fig. 2.3, as long as the two new thermo-junctions are at the same temperature, the net emf of the circuit is unchanged irrespective of the temperature of C away from the junctions.

(3) If metal C is inserted between A and B at one of the junctions as shown in Fig. 2.4, and the temperature of C at any point away from the junctions formed by metals A and C and metals B and C is also at the temperature T_1, then the net emf is the same as if C was not there.

(4) If the thermal emf of a thermocouple formed by metals A and C is E_{AC} and also the thermal emf from that formed by metals B and C is E_{CB} as shown in Fig.2.5, then the thermal emf of a resulting thermocouple formed by metals A and B is $E_{AC} + E_{CB}$

(5) If a thermocouple produces emf E_1 when the junctions are at T_1 and T_2 and E_2 when at T_2 and T_3 as shown in Fig.2.6, then it will produce E_1+E_1 when the junctions are at T_1 and T_3

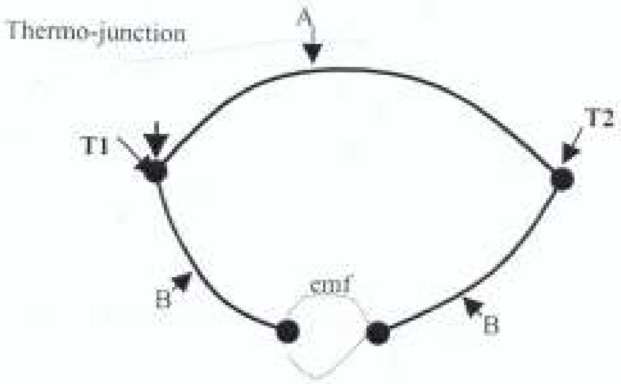


Fig 2.1: A simple thermocouple connection

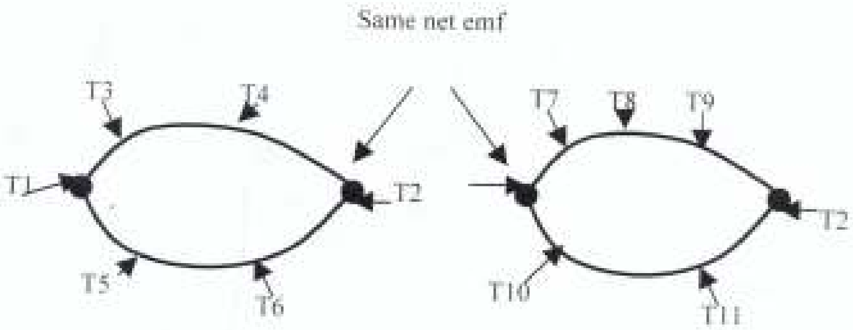


Fig 2.2: Thermocouple with homogeneous materials

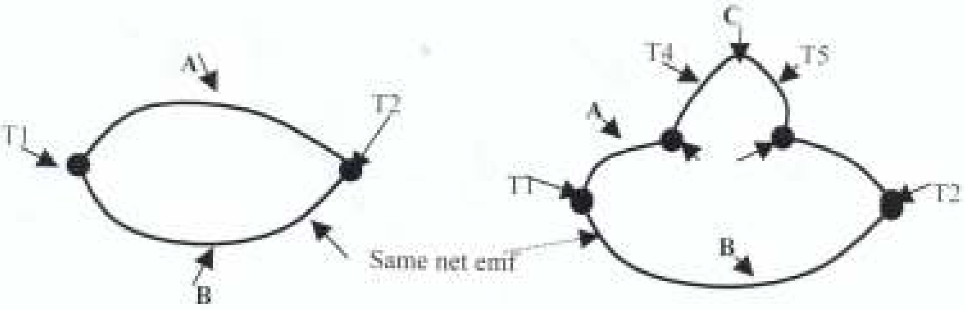


Fig 2.3: Thermocouple with a third material

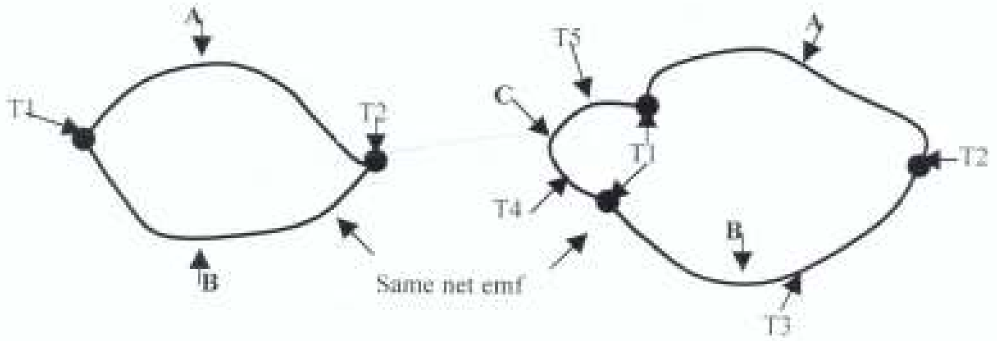


Fig 2.4: The effect of introducing a third material

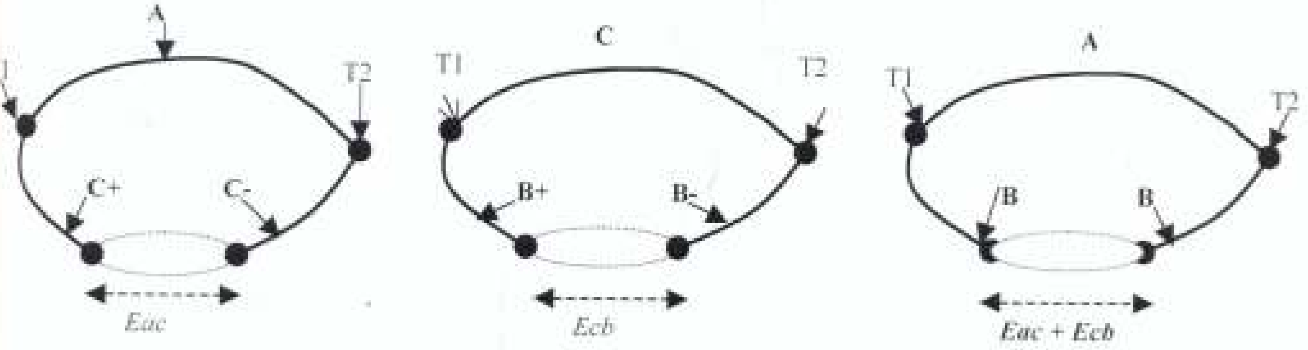


Fig 2.5: Thermal emf produced by different combination of materials

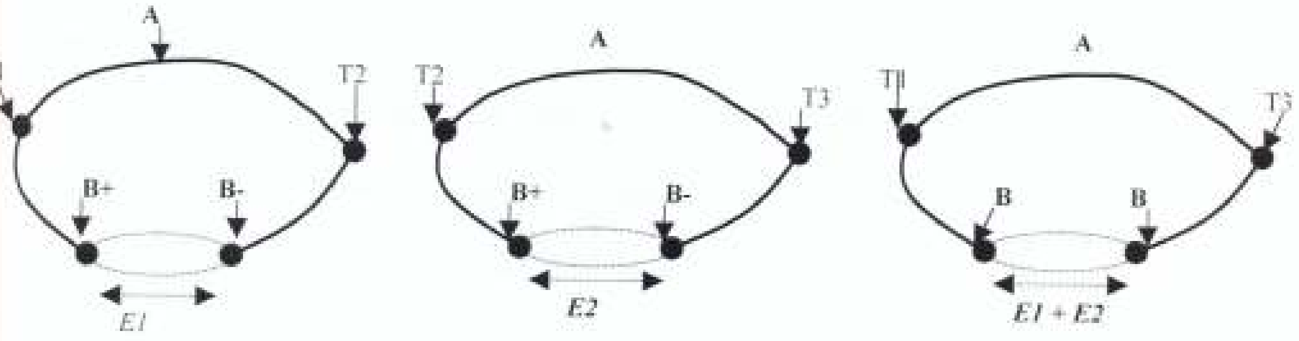


Fig 2.6: Thermal emf generated by thermocouple at different temperature

These laws are of great importance in the practical application of thermocouples. The first law states that the lead wires connecting the two junctions may be safely exposed to an unknown and or a varying temperature without affecting the voltage produced. Laws 2 and 3 make it possible to insert a voltage-measuring device into the circuit to measure the emf. Here the metal C represents the internal circuit (usually all copper in practical instruments) between the instrument binding posts. Law 3 also shows that thermocouple junctions may be soldered or brazed (thereby introducing a third metal) without affecting the readings. Law 4 shows that all possible pairs of metal need not be calibrated since the individual metals can each be paired with one standard (platinum) and calibrated. Any other combinations then can be calculated.

In considering the fifth Law it should be noted that in using a thermocouple to measure an unknown temperature, the temperature of one of the thermo-junctions (called the reference junction) must be known by some independent means. A voltage measurement then allows us to get the temperature of other (measuring) junction from calibrated tables. Most calibration tables are based on reference junction set at the triple point of water. When a thermocouple is used, the reference junction may or may not be at the ice point. If it is, the calibration table may be employed directly to find the measuring junction temperature. If it is not, the fifth law allows the use of the standard table as follows: suppose the reference junction is at 30^0C and the voltage reading in the table is 0.71mV. Now E_2 the measured value is 1.23mV, thus $E_1 + E_2 = 1.94$mV. The unknown temperature can be found by looking up the temperature value corresponding to 1.94mV (Labfacility, 2001).

2.2.2 COMMON THERMOCOUPLE

While many materials exhibit the thermoelectric effect to some degree, only a small number of pairs are in wide use. They are Platinum/Platinum-Rhodium, Chromel/Alumel, Copper/ Constantan, and Iron/ Constantan. Each pair exhibits a combination of properties that suits it to a particular class of application. Since the thermoelectric effect is somewhat non-linear, the sensitivity varies with temperature. The maximum sensitivity of any of the above pairs is about $60\mu V/^0C$ for Copper/Constantan at 350^0C, Platinum/Platinum-Rhodium is the least sensitive, its sensitivity being about $6\mu V/^0C$ between 0 and 100^0C.

The accuracy of the common thermocouples may be classified in two ways, either (1) relying on the wire manufacturer's quality control to limit deviation from the published calibration table or (2), by calibrating individual thermocouple before use. Of all types of thermocouples, Platinum/Platinum-Rhodium is the most accurate; the error is of the order of ± 0.25 percent (Barney, 1988).

Platinum/Platinum-Rhodium thermocouples are employed mainly in the range 0 to 1500^0C. The main features of this combination are its chemical inertness and stability at high temperature in oxidising atmospheres. Reducing atmospheres cause rapid deterioration at high temperature as small quantities of other metals absorbed from nearby objects contaminate the thermocouple metals. This difficulty causes loss of calibration and unfortunately it is a common occurrence in most thermocouple material above 1000^0C. Chromel/Alumel couples are useful over the range –200 to $+1300^0C$. Their main application, however, is from about 700 to 1200^0C in non-reducing atmospheres. The temperature/voltage characteristic is quite linear in this temperature range. Other thermocouples in wide use include Copper/Constantan, used at temperature as low as -200^0C. Its upper limit is about

350°C because of the oxidation of copper above this range. Iron/Constantan is the most widely utilised thermocouple for industrial application and covers the range –150 to + 1000°C. It is usable in an oxidising atmosphere to about 760°C and to about 1000°C in a reducing atmosphere.

2.2.3 REFERENCE –JUNCTION CONSIDERATION.

For the most precise work, the reference junction should be kept at the triple-point of water whose temperature is 0.01± ± 0.0005°C. Such accuracy is rarely needed, and an ice bath is used much more commonly. A carefully made ice bath is reproducible to about 0.001°C. Fig 2.7 shows one method of constructing an ice-bath reference junction. The main sources of errors are insufficient immersion length and an excessive amount of water in the bottom of the flask. Temperature measurement in this case is achieved by looking up the value of the voltmeter reading in a standard thermocouple chart, which is normally referenced at 0°C.

Since low–power heating is obtained more easily than low-power cooling, some reference junctions are designed to operate at a fixed temperature higher than any experienced ambient. A feedback system operates an electric heating element to maintain a constant and known temperature in an enclosure containing the reference junctions. Since the reference junction is not at 0°C, the thermocouple output voltage must be corrected by adding the reference junction voltage to the measured voltage value at the thermocouple terminals. This correction is however a constant.

Fig. 2.8 shows a reference junction technique widely utilised for digital thermometers, data loggers and data acquisition system. Wires from the measuring junction are screwed directly to an isothermal block terminal strip. The temperature of this block (which has no active temperature control) drifts with ambient temperature. This reference temperature is measured by an independent means. Often a junction semiconductor sensor and a compensation circuit develop a voltage E_{comp} that is combined with that from the measuring junction so that the net voltage presented to the voltmeter represents the measured temperature $T_{measured}$.

In a recent development, the compensation and the entire measurement are carried out with the aid of a microprocessor computing power. Due to the increasing interest in high temperature processes in jet and rocket engines and nuclear reactors there is an increasing requirement for a reliable temperature sensor in the range 1500^{o}C to 3500^{o}C. New thermocouple developed for these applications include Rhodium-Iridium/Rhodium, Tungsten /Rhodium and Boron/Graphite. Thermocouples in common use are made from wires ranging from about 1mm to 2mm in diameter, the larger diameters are required for long life in severe environments. Speed of response, conduction and radiation errors and precision of junction location can all be improved by the use of smaller wires.

Several thermocouples may be connected in series or in parallel to achieve useful functions. The series connection with all measuring junctions at one temperature and all reference junctions at another is used mainly as a means of increasing sensitivity. Such an arrangement is called a thermopile and for N thermocouples in series, a d.c. output N times that of a single couple is obtained. The parallel combination generates the same voltage as a single couple if all their hot junctions are set at the same high temperature, and reference junctions are at the same temperature.

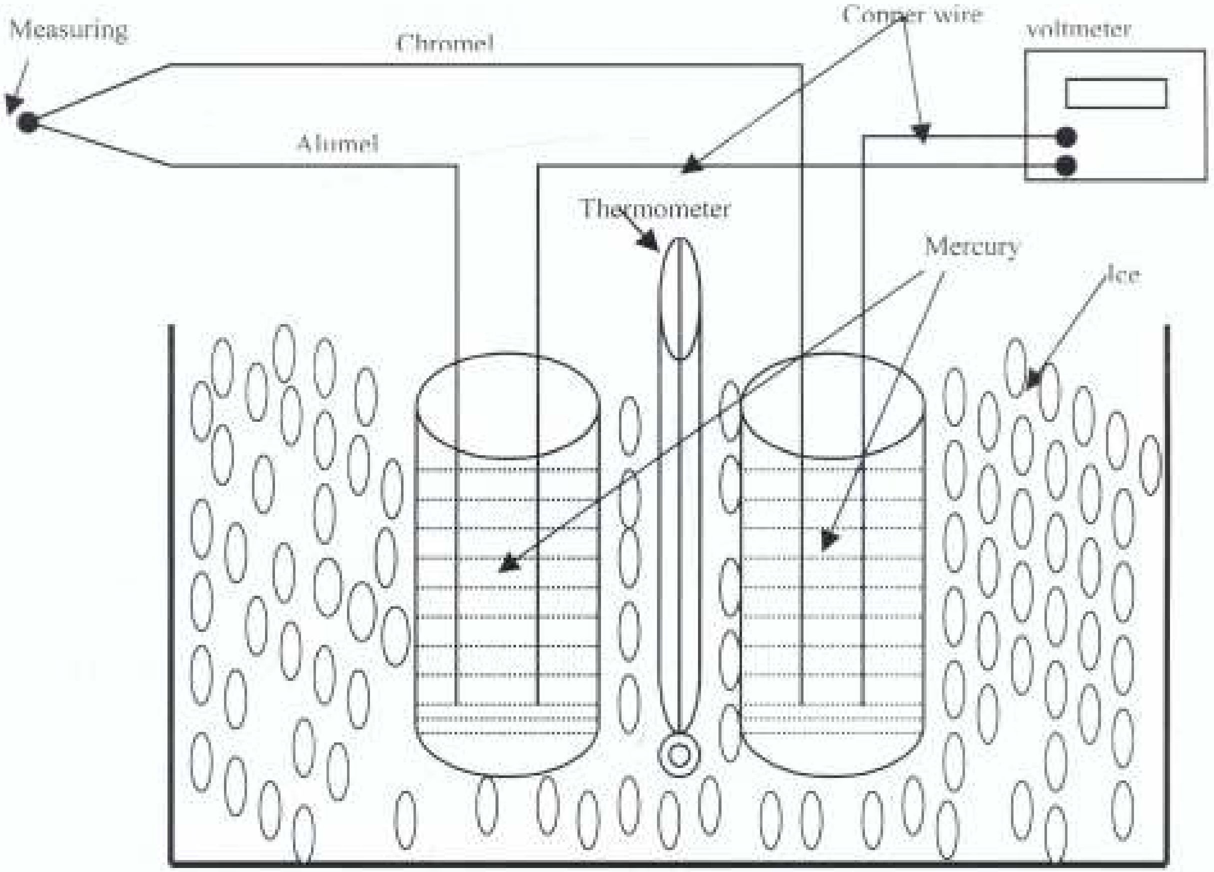


Fig 2.7: Reference junction consideration at 0°C

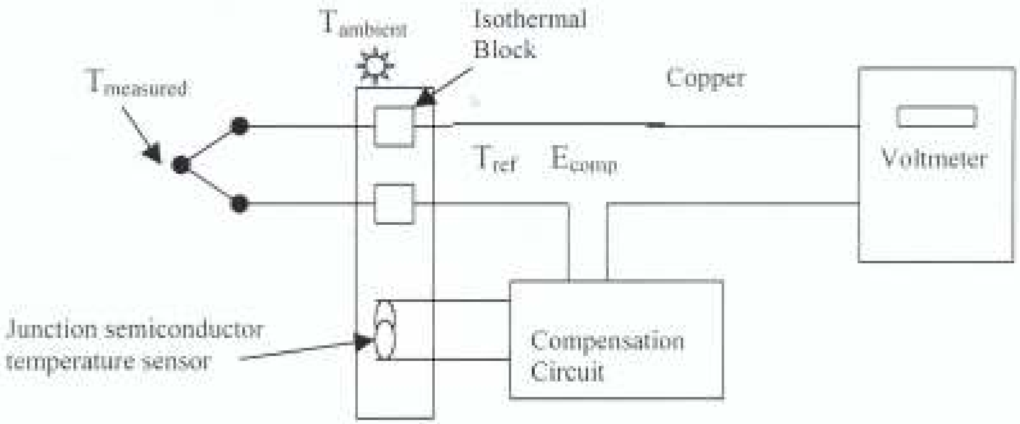


Fig 2.8: Reference junction compensation network

2.2.4 OTHER THERMAL SENSORS,

There are several other types of thermo-sensors in common use today. They include the electrical resistance sensors that are made from material whose electrical resistance varies with temperature and the junction-semiconductor sensors. Junction semiconductor devices such as the diode and transistor are known to exhibit a change in their junction potential with temperature. Sensors of this kind although not commonly applicable in high temperature measurement find application within the temperature range of -55 to $155^{\circ}C$ in non-reducing and non-oxidising environment.

2.3 THERMOCOUPLE AMPLIFIER CIRCUITS

The data generated by a basic measuring device generally require processing or conditioning of one sort or another before it is presented to the observer through an indicator or a recorder. Devices for accomplishing these operations may be specific to a certain class of measuring sensor or they may be quite general purpose. Since the electrical signals produced by most transducers are of low voltage (of the order of a few microvolt), it is often necessary to amplify such voltages before they are suitable for further analogue or digital processing, transmission, or used to drive other devices. The use of op-amp in the construction of amplifiers for transducers of low output voltage is a widely utilised analogue electronic subassembly and it is the basis of instrumentation amplifiers, filters and myriad of analogue and digital data processing equipment. For the basis of this work we shall not be concerned with the electronic details of the op-amps, but simply rely on certain physical assumptions about their behaviour as prescribed in op-amp design and application notes.

The op-amp forms the basis of the circuit design in this project, and since all op-amps have an inherent deviation from ideal, it becomes necessary to analyse the basic operation of the op-amp and the error reduction techniques that can be used in op-amp design in order to get an accurate result. First we discuss the various ideal features of op-amps meant for linear application using feedback and later on the various sources of error and error budget that can lead to a low noise precision op-amp circuit design.

2.3.1 THE IDEAL OP-AMPS

Fig.2.9 shows an ideal op-amp with its major inputs and output terminal. The ideal characteristics of an Op-amp are given by many authors (e.g. Franco, 1988). Below is an outline of some of the important properties:

1. Infinite voltage gain A. $Vout = A(V2 - V1)$ where $A = \infty$
2. Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the preceding stage
3. Zero output resistance R_o, so that output can drive an infinite number of other devices.
4. Output voltage is zero when both $V2$ and $V1$ is zero volt or grounded.
5. Infinite bandwidth so that any frequency from zero to infinite frequency can be amplified without any attenuation.
6. Infinite common-mode rejection ratio so that the output common-mode noise voltage is zero. i.e. the device amplifies only $|V2 - V1|$ the difference in input voltage to the order of 80 - 90dB.
7. Infinite slew rate so that the output voltage change occurs simultaneously with input voltage change

These interesting features are however not present in practical op-amps. A practical op-amp can be made to work close to an ideal by the introduction of a negative feedback arrangement. The next section discusses the various sources of error in op-amp circuitry and the various processes used in practice to increase the effectiveness of op-amp based amplifiers.

2.4 PRECISION DESIGN AND ERROR BUDGET

The ideal characteristics of op-amp described in last section are usually not present in practical op-amp circuit. The practical op-amp has an inherent d.c. output voltage, called output offset voltage when both inverting and non-inverting input terminals are grounded. Such an output voltage is an error voltage and is therefore undesirable.

Errors in linear op-amp circuits can be divided into three main categories:

(a) Op-amp errors associated with the input circuitry

(b) Op-amp error associated with the output circuitry

(c) Errors in the external network component

2.4.1 OP-AMP INPUT ERRORS

The deviations of most op-amp's input characteristics from the ideal generally constitutes serious obstacles to precision circuit design, and forces trade off in circuit configuration, component selection and the choice of op-amp type. The finite value of input impedance, input current, voltage offset, common-mode rejection ratio, power supply rejection ratio and their drift with time and temperature are all sources of a cumulative error introduced in circuit using op-amps as the basis.

2.4.1.1 INPUT BIAS CURRENT

An input bias current I_B is defined as the average of the two input bias currents I_{B1} and I_{B2} as shown in Fig.2.10 (a) i.e.

$$I_B = \frac{I_{B_1} + I_{B_2}}{2} \tag{2.2}$$

Where I_{B_1} is dc bias current flowing into the non-inverting.

I_{B_2} is dc bias current flowing into the inverting input.

Given that both inputs are grounded so that the net input voltage is zero, the input bias currents I_{B_1} and I_{B_2} are the base currents of the two transistors in the input differential amplifier stage of the op-amp. Although both input transistors are identical it is not possible to have I_{B_1} and I_{B_2} exactly equal. This input bias current, although in the range of a few hundred nanoamperes, can cause a significant output offset voltage in circuit where relatively large feedback resistors are employed.

For an inverting amplifier as shown below in Fig.2.10 (b), the offset caused by the input bias current is given by

$$V_{offset} = R_f I_B \tag{2.3}$$

And it becomes significantly large with a large feedback resistor R_f. In order to reduce the effect of such input bias current we use an op-amp with low input bias current. Op-amps with FET transistor inputs in the differential pair are a very good choice because of their inherent low input bias current, however most op-amps have provision for the offset voltage to be nulled, what matters more is the drift with temperature. In this case FET amplifiers are 3 to 6000 times worse than bi-polar op-amps such as the OP-07 and OP77.

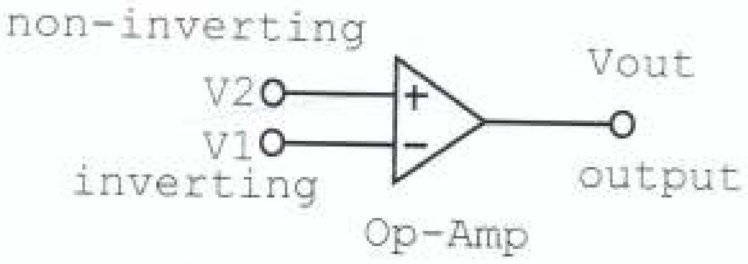


Fig.2.9: General symbolic representation of an op-amp

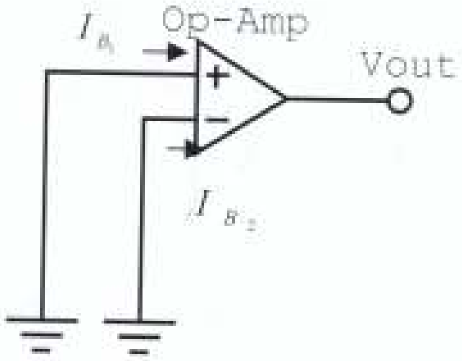
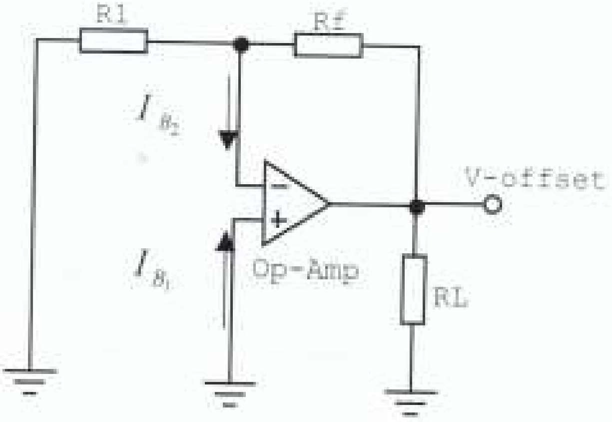


Fig 2.10 (a): Input bias current of op-amps with the inputs grounded



(b): Offset voltage due to input bias current in non-because their input bias current rises drastically with increasing temperature. It roughly doubles for every 10^oC, whereas for a bipolar input op-amp, the input bias current which is basically base current, drops with temperature rise (Horrowitz, 1995).

2.4.1.2 INPUT OFFSET VOLTAGE

Input offset voltage V_{io} is the differential voltage that exists between two input terminals of an op-amp without any external input applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero. There exists an output-offset voltage V_{oo} as a result of V_{io} which results from a mismatch in the two input terminals even though all the components are integrated on the same chip. This output voltage V_{oo} is either positive or negative in polarity depending on the polarity of V_{io}.

To reduce the output offset voltage V_{oo} to zero therefore; we need to have a current at the input terminal of the op-amp that will give the flexibility of obtaining V_{io} of proper amplitude and polarity. Such a circuit is called an input-offset voltage compensation network. Although most single op-amp have offset adjustment terminals as mentioned earlier, it is wise to choose an op-amp with an inherent low initial offset voltage max V_{os}. Firstly, an op-amp with low initial offset voltage tends to have a corresponding low offset drift with temperature. Secondly a sufficiently precise op-amp eliminates the need for external trimming components, and thirdly, offset voltage and common-mode rejection ratios in most practical op-amps are degraded by unbalances caused by potentiometers normally employed in offset nulling (Franco, 1988).

Because the voltage offset can be trimmed to zero what ultimately matters is the drift of offset voltage with time, temperature and power supply voltage variation. Manufacturers of precision op-amps therefore employ various improved design processes to minimise sources of errors. Bipolar op-amp like the LM308 or OP-07 are a good choice, the best so far advertised to cope with this problem is the AD707 claiming the smallest drift $\Delta V_{os}=0.1\mu V/^{0}C$ (max).

Another factor to keep in mind is the drift caused by self-heating of op-amp when it drives a low impedance load. It is often necessary to keep the load impedance above 10kΩ to prevent large errors from this effect.

2.4.1.3 COMMON-MODE REJECTION ERROR

Insufficient common-mode rejection ratio (CMRR) degrades circuit precision by effectively introducing a voltage offset as a function of dc level at the input. This effect is usually negligible since it is equivalent to a small gain change, and in any case it can be overcome by the choice of circuit configuration. For example an inverting amplifier is insensitive to op-amp CMRR. In contrast to this, in non-inverting amplifier applications the signal between the input terminals is a small differential signal ridding on a large d.c. voltage, and thus a high CMRR is essential.

2.4.1.4 POWER SUPPLY REJECTION

Variations in power supply voltage causes small op-amp errors, as with most op-amp specification the power supply rejection ratio (PSRR) is considered to be a signal at the input and it does add up to the real input signal. For example the OP77 has a specified PSRR of 110dB at d.c. meaning that a 3.0V change in one of the power supply lines causes a change at the output equivalent to a change in differential input signal of 1μV. Hence the use of regulated power supply has become a part of most precision circuit design. The 78XX and 79XX positive and negative voltage regulators respectively are recommended.

2.4.2 OP-AMP ERROR DUE TO OUTPUT CIRCUITRY

As discussed earlier when an op-amp is driving a low impedance load, self-heating occurs in the op-amp and thus results in the op-amp characteristics varying in some cases rapidly. Other serious limitations associated with the output stage are limited slew rate, output crossover distortion and finite open-loop output impedance, which are the predominant sources of error in alternating voltages op-amp application. It is therefore a good design technique to always ensure that op-amp circuits are terminated with high impedance devices, and if the need arises to use it as a driver for low impedance loads then it should be terminated with a suitable unity buffer.

2.4.3 COMPONENT ERRORS

The degree of precision of circuits used for generating reference voltages, current sources, e.t.c. depends to a large extent on the accuracy and thermal stability of the resistors used in the external networking. The common mode rejection ratio of a differential amplifier for example is known to be greatly affected when the ratios of the two pairs of resistors used at the differential inputs do not match. In the same vane, the accuracy and linearity of the ramping action of integrators is also largely dependent on the properties and stability of the capacitor used in the circuit. Therefore the choice of components is vital in any circuit implementation.

Components are generally specified with an initial accuracy, as well as the changes in value with time and temperature. Complete specification also includes the effect of temperature cycling and soldering, shock and vibration, short-term overload and moisture. The table 2.1 gives the specification for the commonly used two resistor types (Horrowitz, 1995). From these specifications it is obvious that for precision work it is necessary to use metal film resistors rather than carbon composition resistor.

Table2.1: Example of variation of resistor properties

Material	**Temperature Coefficient (Tempco)**	**Soldering Temperature and Load Cycle**	**Shock and Vibration**	**Moisture**
Metal film Resistor	50ppm/°C	-55°C to 175°C	0.1%	0.5%
5%Carbon composition Resistor	80ppm/°C	25°C to 85°C	2%	6%

2.5 DATA TRANSMISSION, MANIPULATION AND RECORDING

When the components of a measurement system are located remotely from one another, it becomes necessary to transmit information between them by some sort of communication channel. In some cases signal transmission problem arises because of relative motion of one part of a system with respect to another. Some of the basic means of signal transmission employed for measurement purposes today are discussed in the subsequent section.

2.5.1 CABLE TRANSMISSION

Perhaps the most common way in which analogue and digital signals are being transmitted is via cable network from one location to another. For analogue signals the reliability of cable as a means of transmission is limited by distributed parameters, since the properties of resistance, inductance and capacitance are not lumped or localised. In this work emphasis will be laid on the hardware rather than the mathematical analysis of the various parameters involved.

A popular device employed in process industries for signal transmission is the so-called current loop transmitter, which converts thermocouple and Resistant Dependent Thermocouple's (RDT) output voltages into proportional output current. For this device a zero input signal produces a minimum current

of 4mA and a full scale input produce 20mA which is transported to the measuring device or indicator through copper wires. Such transmitters are available in several forms, the two wire version is shown below in Fig 2.11 is in particular convenient because of its ability to maintain a constant current for a given voltage input for the entire length of its transmission line. When data must be transmitted over very long distances, analogue signals tend to be corrupted by the response characteristics of the transmission line. It is therefore desirable to convert the analogue signal into a digital form and thereafter it is either frequency modulated or frequency shift-keyed through the transmission line to be demodulated at the receiving end.

2.5.1 FIBER OPTICS DATA TRANSMISSION

Of increasing interest today is the use of optical rather than electrical means of signal transmission. And it is now used for both analogue and digital transmission of signals. Basically an electrically controllable light source usually Light Emitting Diodes (LED), an optical fibre, and a photo-detector are the components that are required. Among the advantages produced by the use of fibre optics as a means of data transmission are its wide bandwidth and high data transfer rate while avoiding many of the interference's associated with electrical means of transmission. Optical fibres are also immune to electromagnetic interference from source such as lighting or power switching and produce good noise rejection. The only limitation of this means of transmission has remained its high cost (Marrangoni, 1993).

2.5.3 FM RADIO TELEMETRY

In many cases of transmission of signal from one place to another interconnecting wire may not be possible. In such cases data may be transmitted by radio. The word telemetry simply means measurement at a distance and includes all forms of such system, opto-telemetry and radio telemetry being the most widely utilised. Considerable standard has been set for the use of radio for data communication. A special frequency band has been allocated based on the requirement of such systems used in telemetry (Mie, 1997).

Figure 2.12 shows the widely utilised system of radio telemetry. The FM/FM refers to the fact that two frequency modulation processes are employed. In the first process, a time varying dc voltage is converted to proportional frequencies by using a voltage to frequency converter. The standard FM/FM system allows for multiplexing of various inputs from different transducers and then transmitted via a single carrier frequency as illustrated in the block diagram. The standard carrier frequency for telemetry is specified from the range 216 to 235MHz.

A digital form of telemetry, the pulse code modulation (PCM) technique is also in wide use. Radio telemetry is very useful over short distances when the relative motion of the measuring device and the readout equipment prevents a suitable direct connection. Examples of such situation are found in measurement on rotating machinery, (for the purpose of this research on a rotary furnace) where a slip-ring technique is not very accurate. Apart from radio telemetry it is important to mention that other means of transmission of data such as, pneumatic transmission, synchro-position repeater systems and rotary transformers are also employed in other areas such as mechanical power transmission (Marrangoni, 1993).

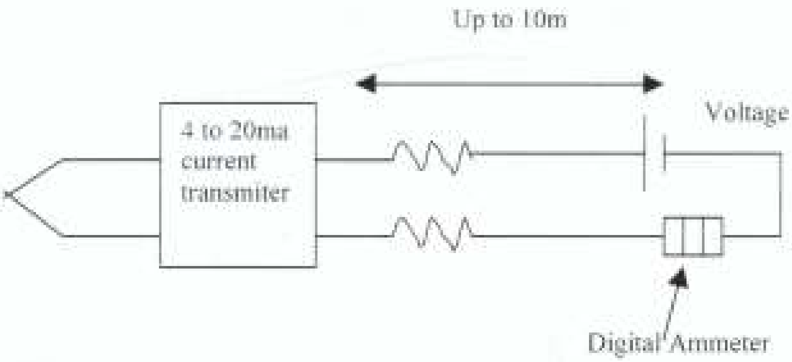


Fig 2.11: A common thermocouple amplifier current

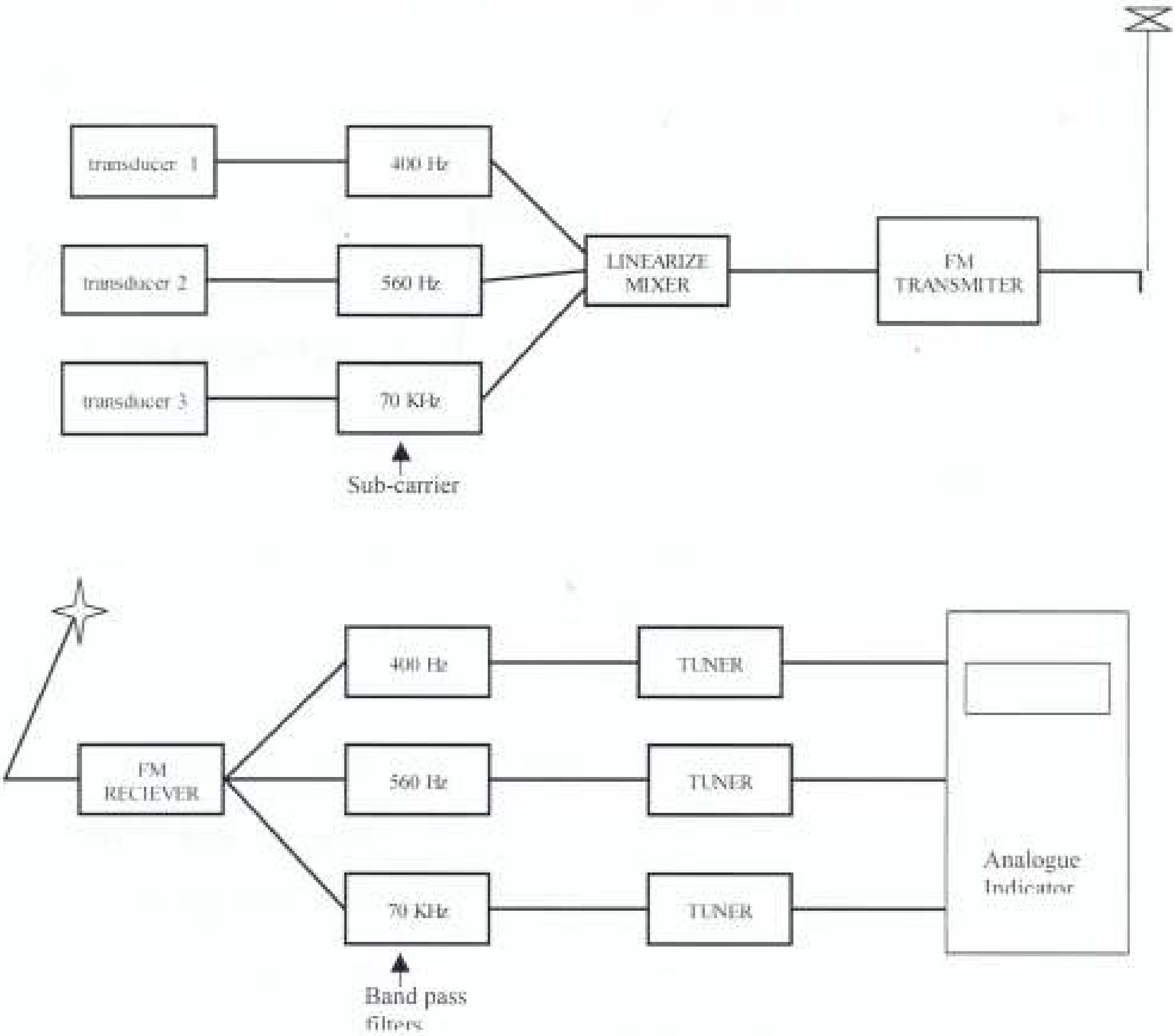


Fig 2.12: A typical FM/FM telemetry system used in multiplexed

2.5.4 DATA MANIPULATION

Various means have been developed by which a signal is manipulated or conditioned before it is finally available to the observer as read out. The basic data manipulating devices relevant to this work are electronics filters, integrators, differentiators and comparators which are discussed section 2.5.4.1

2.5.4.1 FILTERS

Filters in signal transmission and reception are used basically as frequency selective devices to pass signals within a desired frequency range and reject signals outside the range. Filters may take various forms depending on the type and frequency range it is expected to filter. Of common use are the mechanical and electrical filters. Electronic filters fall into four main groups namely the low pass, high pass, band pass and the band reject filters.

2.5.4.1.1 Low pass filter

The ideal low pass filter passes signals in the form of alternating emf whose frequency lies between 0 Hz up to a fixed limit $f_{H\ max}$ All other frequencies above this limit is however not passed. A practical low pass filter on the other hand passes frequency at constant amplitude up to a frequency usually referred to as the 3dB point for which all other frequencies suffers significant amplitude attenuation. Fig. 2.13 shows the action of both an ideal and a practical low pass filter on a signal of varying frequency.

2.5.4.1.2 High pass filter

A high pass filter on the other hand passes signal frequency above a fixed minimum frequency F_L The characteristic difference between an ideal high pass filter and a practical one is also demonstrated in Fig. 2.14. The filter has a 3dB point after which the amplitude of transmitted signal is maintained constant (only for Butterworth filters).

2.5.4.1.3 Band pass filter

The band pass filter can simply be achieved by cascading a low pass and a high pass filter in series. It allows frequencies that fall within the frequency band $f_1 < f_o < f_H$ set by the 3dB limits of both filters to pass and attenuate all other frequencies below f_1 or above f_H. The frequency range $f_H - f_l$ defines the bandwidth of the filter. Many band pass filter designs exist and the choice of a particular type is almost dictated by the requirement of the filter, such as ripple rejection and the attenuation span (Franco, 1988).

2.5.4.1.4 Band reject filter

Band reject filter passes all frequencies except a set frequency f_R, which it attenuates significantly. The diagrams on Fig. 2.15 demonstrate both filter characteristics.

Filters can be constructed using discrete components such as capacitors, resistors and inductors, such filters are referred to as passive filters. Passive filters are still very much in wide use because of their inherent low noise, require no power supplies and have a wide dynamic range. Modern filters generally include transistors, op-amps and other active devices and are thus referred to as active filters. Active filters however find a dominant application environment because they are much more adjustable. They have a very wide frequency range, very high input and very low output impedance that makes cascading and interconnection a simple task. The frequency selectivity of any of the filters depends on the design configuration and the filter order, and for the band pass and band reject it also depends on its quality factor which also specifies the bandwidth.

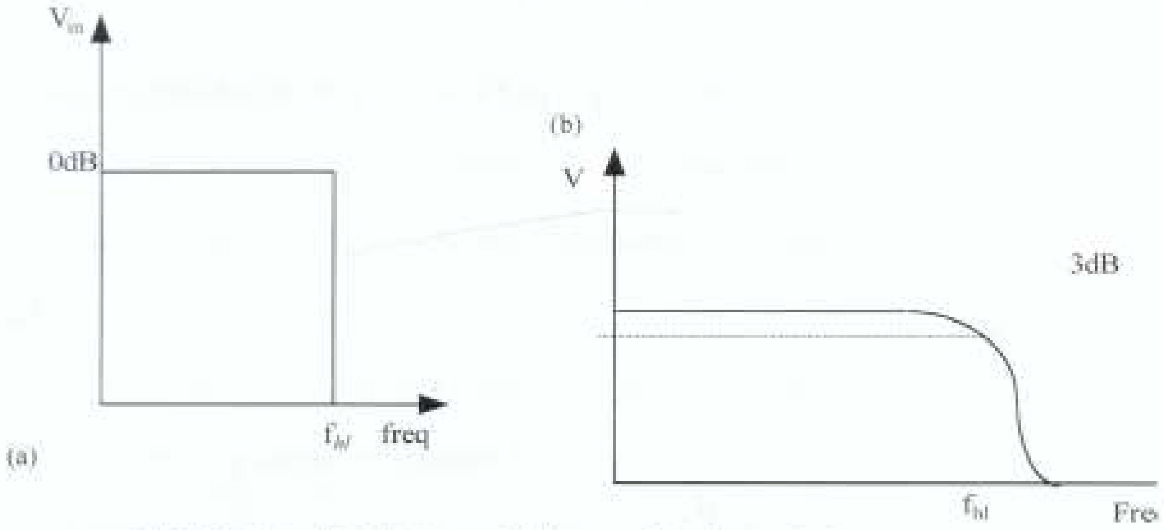


Fig.2.13: (a) An ideal (b) A practical low pass filter characteristics

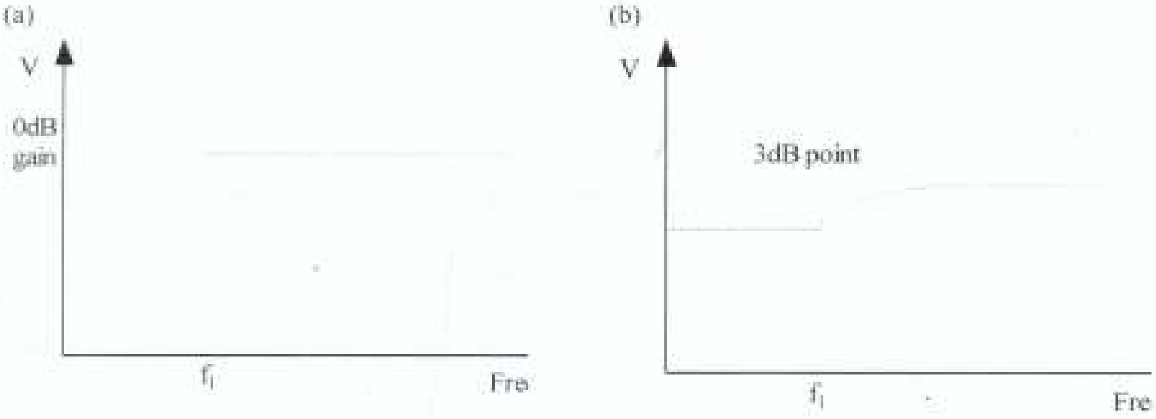


Fig.2.14: (a) An ideal (b) A practical high pass filter characteristics

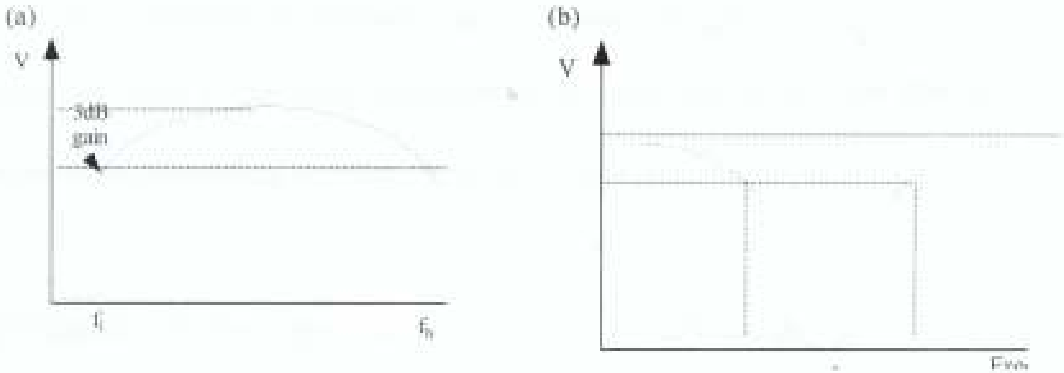


Fig.2.15: (a) Band pass (b) Band reject

2.5.4.2 INTEGRATION AND DIFFERENTIATION

Often in electronics measurement it is necessary to obtain the integral or the derivative of a signal with respect to time, depending on the physical nature of the signal.

2.5.4.2.1 The integrators

The circuit in which the output voltage is the integral of the input voltage is an integrator. Such a circuit is obtained by using a basic inverting amplifier configuration in which the feedback resistor R_f is replaced by a capacitor C_f as shown in Fig. 2.16

The expression for the output voltage V_o is given by

$$V_o = \frac{-1}{R_1 C_f}\int_0^t V_{in}\partial t + v_{io} \qquad (2.4)$$

where v_{io} is the integration constant and is proportional to the value of the output voltage V_o at time $t = 0$. Fig. 2.17 shows the input and output waveform response of an integrator to both a square wave and a sinusoidal wave.

2.5.4.2.2 The differentiator

The differentiator performs the mathematical operation of differentiation i.e. the output waveform is the time derivative of the input waveform. The differentiator can be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1

The expression for the output voltage can simply be expressed as

$$V_o = -R_f C_1 \partial V_{in} / \partial t \qquad (2.5)$$

Hence the output V_0 is equal to $R_f C_1$ times the negative instantaneous rate of changes of the input voltage V_0 with time. Fig. 2.18 shows a typical circuit arrangement for a simple differentiator amplifier and Fig. 2.19 is the input and output waveform of a differentiator at a given frequency. Sine wave input results into cosine and square wave into positive and negative spikes. The basic application of integrators and differentiators are in the generation of ramp waveforms and in phase shifter.

2.5.4.3 COMPARATORS

A comparator as used in electronic instrumentation compares a signal voltage on one input of an op-amp with a reference voltage on the other input. In its simplest form it is nothing more than an open loop op-amp with two input signals, one at the inverting input and the other at the non-inverting input. The output of the comparators may go positive saturation or negative saturation depending on which of the input voltages is the larger. Comparators have a digital output. They are used in circuits involving digital interfacing, Schmitt triggers, discriminators, voltage level detectors and oscillators.

Fig. 2.20 shows how an op-amp can be used as a comparator. A fixed reference voltage V_{ref} of 1V is applied to the inverting input, and a time varying signal voltage V_{in} is applied to the non-inverting input. For this arrangement the circuit is called the non-inverting comparator. When V_{in} is less than V_{ref}, the output voltage V_0 is at $-V_{sat}$ because the voltage at the (-) input is higher than at the (+) input. When V_{in} is greater than V_{ref} , V_o goes to $+ V_{sat}$ ($=+V_{cc}$). Thus V_0 changes from one saturation level to another whenever $V_{in} = V_{ref}$ as shown in Fig 2.21.

The important characteristics considered in circuit design with a comparator are these (a) speed of operation (b) accuracy (c) compatibility of output with other devices

The output of the comparator must switch rapidly between saturation levels. This implies that the bandwidth of the comparator must be rather wide. The speed of operation of the comparator is improved with positive feedback. The accuracy of the comparator depends on its voltage gain, common-mode rejection ratio, input offset and thermal drift. The high voltage gain allows the comparator to respond to a smaller differential voltage at its inputs.

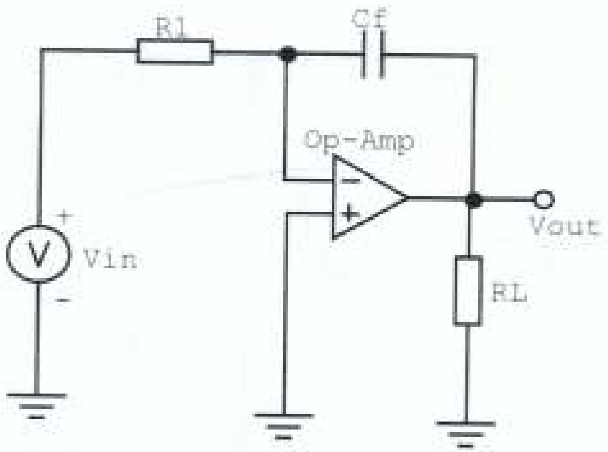


Fig.2.16: An integrator circuit with the feedback resistor replaced by C_f

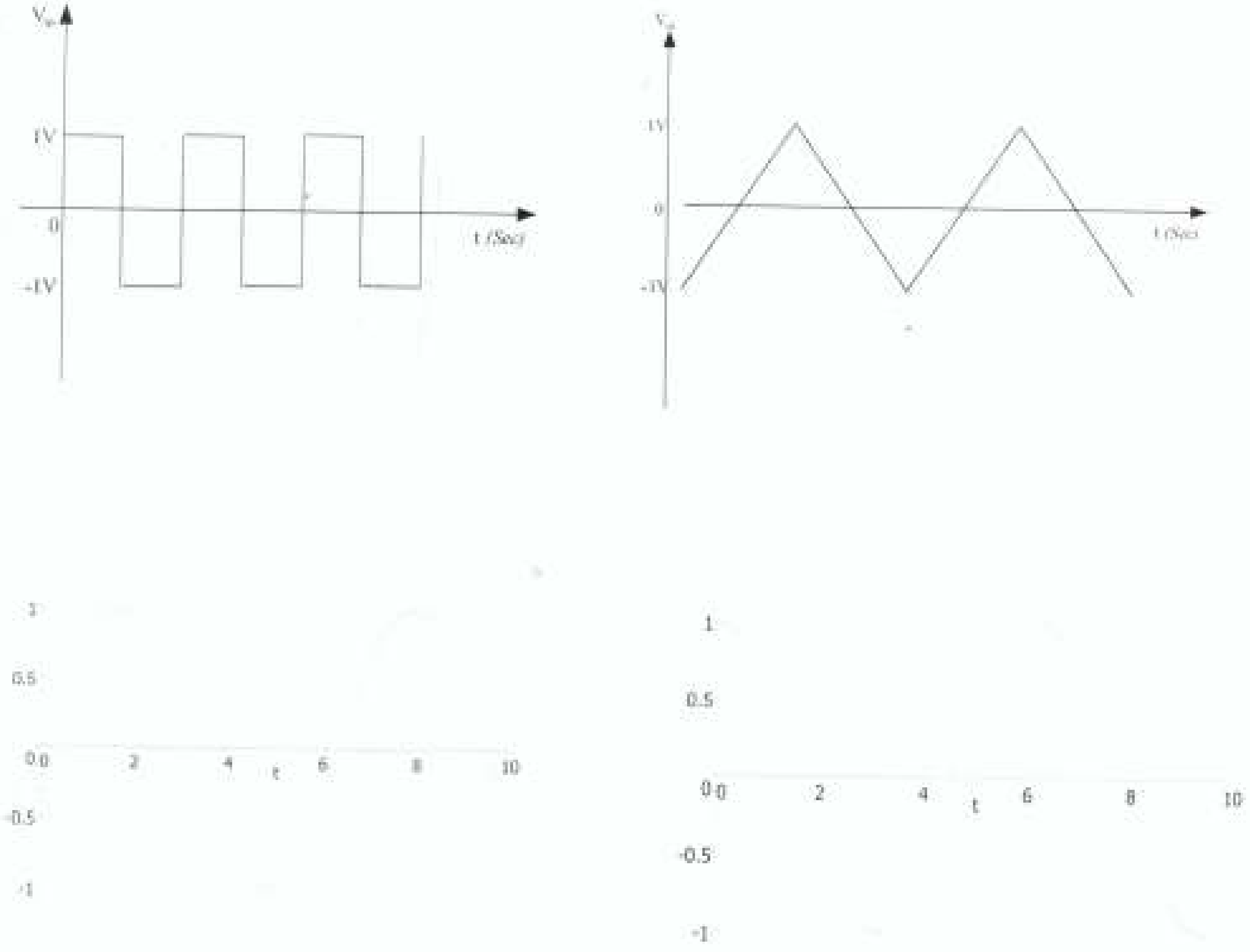


Fig.2.17: Characteristics input and output waveform of an integrator

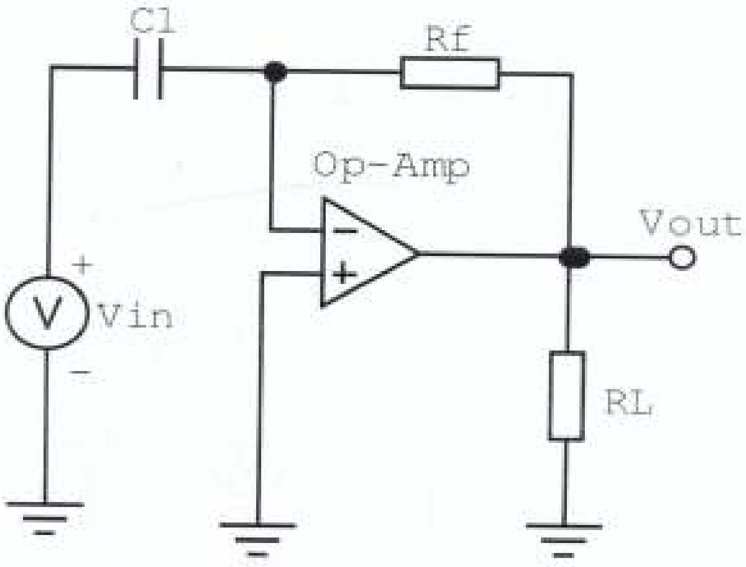


Fig.2.18: A typical differentiator circuit with the input resistor replaced by C_f

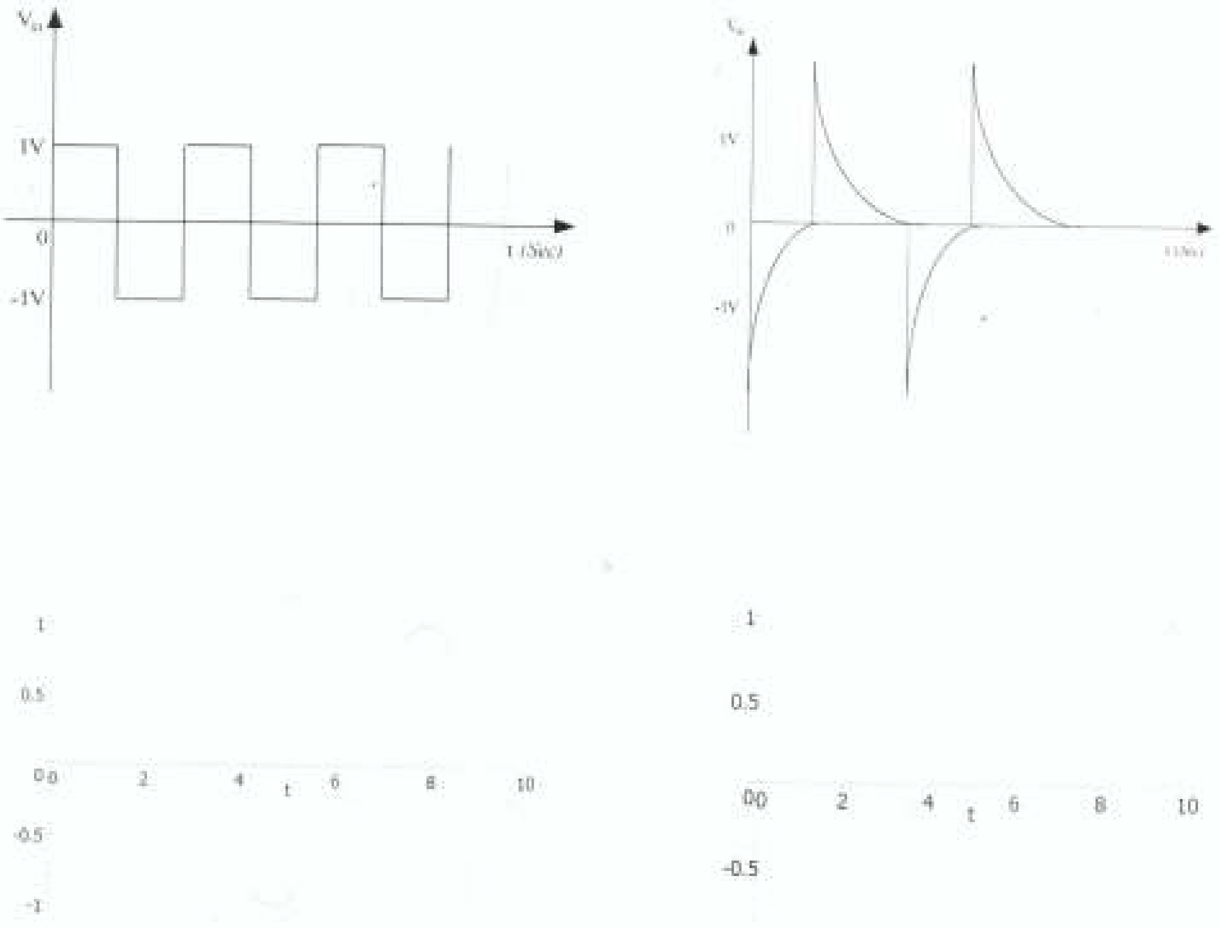


Fig.2.19: Characteristics input and output waveform of a differentiator

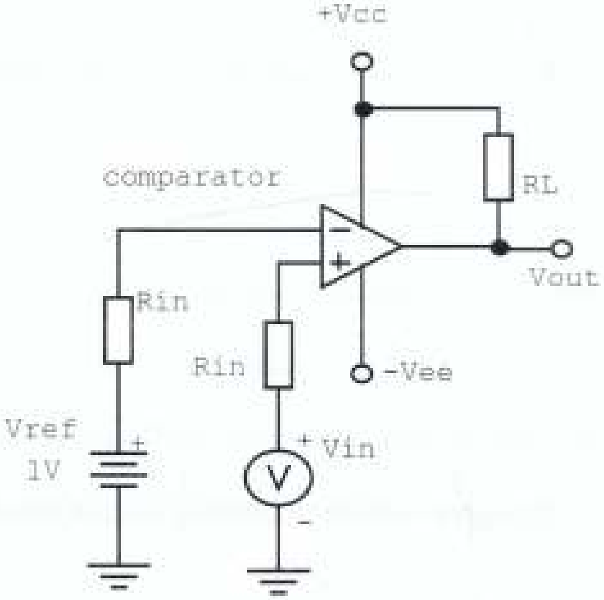


Fig.2.20: A typical comparator circuit with reference voltage at 1V

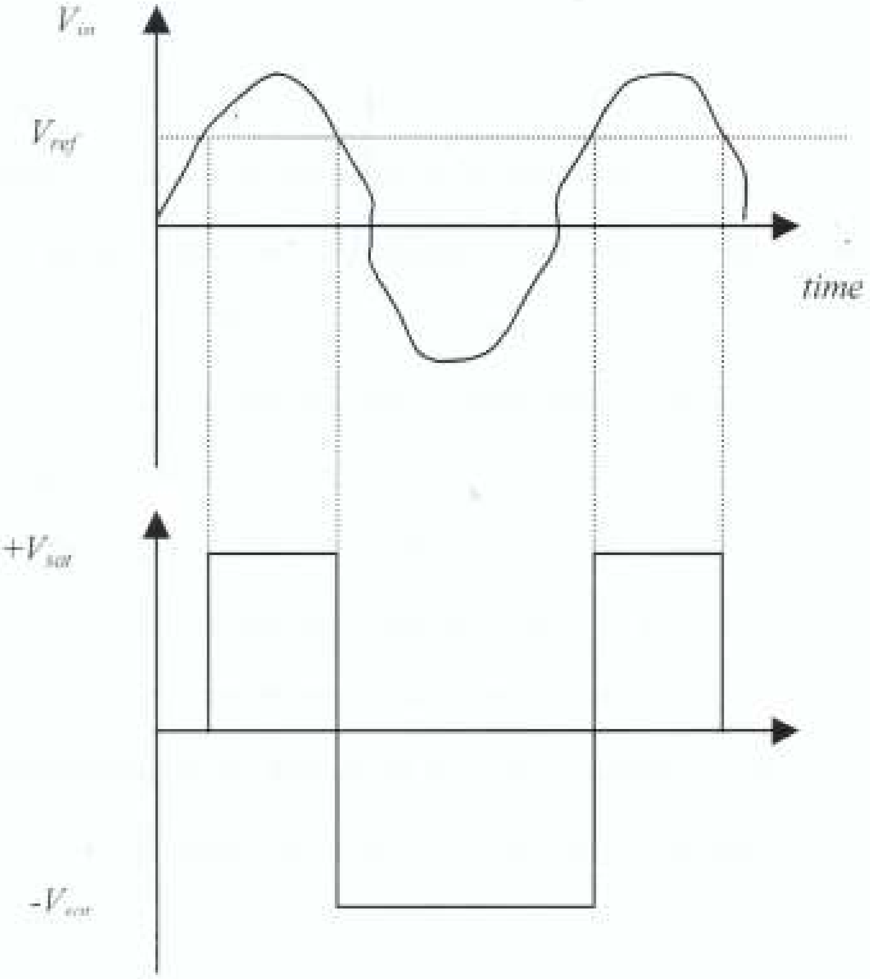


Fig.2.21: Input and output waveform for a comparator

while the high CMRR helps to reject the common-mode input voltages and thus makes it immune to noise at the inputs.

Comparators are a vital component in analogue-to-digital converter circuits, in such cases its output is made to swing between two logic levels suitable for digital interfacing. There are many comparators I.Cs available in the market today. One type is the LM311 (single) and LM339 (quad). They are widely used because their outputs are of the open collector type and thus making it possible to make it compatible to any logic IC family.

2.5.4.4 FUNCTION GENERATION AND LINEARISATION

The majority of indicating devices used for measurement operate in a linear mode, but unfortunately most transducers are generally non-linear. In order for us to have a linear representation of the measured quantity on the read-out, there should be a form of linearisation. Various techniques have been developed for linearisation, ranging from the non-linear potentiometer used as multiplier/divider and the diode function generator (Webb and Greshock, 1993). Multiplier/dividers and multi-fraction modules provide a smooth approximation to the desired function. A diode function generator, which is an alternative approach, gives a piecewise linear curve fit.

A thermocouple generally suffers from non-linearity; therefore different types of linearisation circuit have been developed. Because of the inherent programmability of today's computers, digital computers provide the most comprehensive, accurate and versatile means for function generation and thus digital linearisation method found useful application in this work. However, in terms of speed of conversion, their speed generally cannot match that of analogue linearisers.

2.5.5 CONVERTERS

Digital systems are used increasingly in many applications because of their increasing efficiency, reliability and economical operating cost. With the development of the microprocessor, data processing has become an integral part of various systems. Data processing involves the transfer of data to and from the microcomputer via input/output devices. Since a digital system uses a binary system of ones and zeros, the data input into the microcomputer have to be converted from analogue form to digital form. The circuit that performs this conversion is called an analogue to digital (A/D) converter. On the other hand, a digital-to-analogue converter (DAC) is used when a binary output from a digital system must be converted to an analogue voltage or current. For this work the concentration was on analogue to digital conversion process.

2.6 DATA INDICATION AND RECORDING DEVICES

The majority of signals in measurement systems ultimately appear as voltages. Since a voltage cannot be seen, it must be changed to a form intelligible to a human observer. The forms in which data are presented generally include a pointer moving over a scale, pen writing on a chart. It includes light beam writing on a photosensitive paper, electron beam writing on a cathode-ray tube, visual presentation of a set of ordered digits and print-out of digital data by a printer. We consider two types of such indicator in common use today.

2.7. ANALOGUE VOLTMETERS AND POTENTIOMETERS,

While digital voltmeters are very popular, analogue meters is still the preferred choice for certain applications. The most widely employed meter movements for d.c. and a.c. measurement in electronics is the classical D'Arsonval meter. This current sensitive device is used to measure voltage by passing the current through a D'Asonval meter and a large resistor maintaining constant by means of some compensating techniques. An electronic voltmeter utilises the D'Arsonval meter but precedes it by an amplifier circuit. The amplifier increases the input impedance and overall sensitivity. The instrument accepts a wide range of d.c. and a.c. input voltages and has a measurement error of 1 to 3 percent at full scale. When an a.c. voltage is to be measured with a D'Arsonval meter, it is necessary to convert the signal from a.c. to d.c. It is common practice to calibrate the scale of the meter to read root mean square values. When an extremely accurate measurement of d.c. voltage is required, a potentiometer rather than a deflecting meter is employed. The potentiometer is a null balancing instrument in which the unknown voltage is compared with an accurate reference voltage, which can be adjusted until the two are equal. Since at the balance point no current flows, error due to IR drop in the lead wires is eliminated. Such IR drop is usually present when a D'Arsonval meter is used to measure dc directly. Fairly common are inexpensive potentiometers, which can give result to the nearest microvolt.

2.8 THE DIGITAL COMPUTER AS A MEASURING SYSTEM TOOL

Small computers either dedicated or general purpose, are a natural adjunct to a measuring system. The computer's connection to the outside (its ports) are generally bi-directional. That is, they may either receive or output data, but only in a well-defined and orderly manner. The computer must be informed through software whether a particular port is to handle incoming or outgoing information. Software assignment of port function is often called configuring the ports. A single line may be all that is required for handling simple limit switch/warning-light information, but multiple lines may be needed for processing analogue-converted inputs. In addition, the input/output data may be handled in either serial or parallel form (Barney, 1988).

2.8.1 THE MICROPROCESSOR

The heart of a microcomputer is in the central processing unit (CPU), or microprocessor unit (MPU). Basically it serves as the control centre for directing the flow of digitised data. It is more than a traffic controller because it not only provides the organisational plan for the flow of information but also assigns the pathways, and can perform unlimited manipulation of the traffic. It accepts inputs as either data or command instructions in digital form, and routes them to predetermined (programmed) destinations over busses (pathways) to displays, memories, controllable devices, etc. Sources of data or commands may be external memories, keyboards, transducers, and so on.

There is a wide range of CPUs available with many levels of complexity, 4-bit, 8-bit, 32-bit and so on. The CPU selected for a given purpose depends on the application. While a 4-bit CPU is enough for a low-end dedicated controller, a 16-bit or 32-bit CPU is selected for general-purpose or high-end microcomputer applications.

Fig. 2.22 is a highly simplified schematic diagram of the external connection and some of the internal features of a typical microprocessor unit Motorola 6800 (Marrangoni, 1993). The diagram shows the primary buses into and out of the processor plus some essential internal devices. To be functionally useful, the system requires additional supporting circuitry external to the CPU, including interfacing devices sometimes referred to as buffers, input/output (I/O) facilities, synchronising clocks, etc.

Various control and decode lines, bus synchronisation, closely akin to multiplexing-demultiplexing, is controlled through the use of two external clock signals. Additional lines are shown, their titles in many cases provide clue to their function

Fig 2.22 shows the following:

1. An address bus consisting of 16 parallel lines for accessing 65,536 different memory locations. The actual number available is of course, dependent on what may be provided by the supporting hardware.
2. A data bus consisting of eight bi-directional lines for simultaneously handling of 8-bit (one byte) of data. This is a two-way street, the direction of flow being controlled by gating eight bits, which provide for 256 combinations.

The figure also shows some of the internal structure of the 6800 CPU. Various registers are used. These may be considered as temporary storage bins for data, instructions, or addresses as they are being shuffled from one location to another. Essentially all data and instructions must pass through one of the accumulator, A or B, each having a one byte (8-bit) handling capacity. Primarily for providing manipulation of 2-byte (16-bit) addresses, the index register, program counter, and stack pointer are added.

The stack consists of the register and its contents are stored in contiguous addresses. The purpose of the stack pointer is to keep track of where the stack information is stored in the external random access memory (RAM). The programme counter controls the sequence of any programme steps, including the starting point. The index register, in addition to other functions provides a channel through which two byte addressing may be handled in a programme.

The arithmetical logic unit (ALU) has a relatively limited capability of manipulating number. It can add one byte to another, determine their difference or it can determine several logic functions such as AND, OR, and EX-OR. To handle data in magnitude requiring several bytes, the Add and Subtract functions of the ALU may involve carryover (for addition) or borrow (for subtraction). It is the function of the status register to monitor such requirement for possible further programme use.

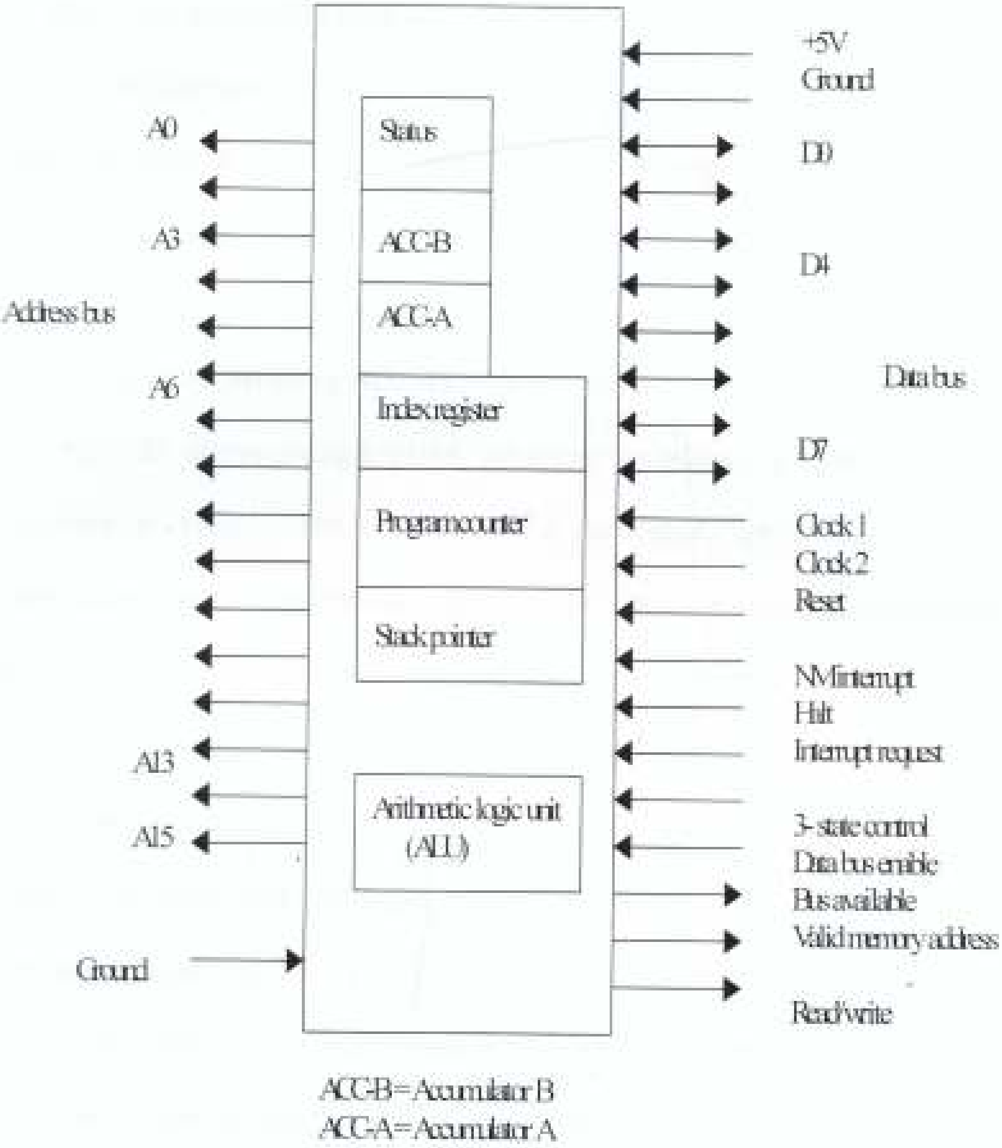


FIG.2.22: The Motorola 6800 MPC unit

2.8.2 THE MICROCOMPUTER

A microprocessor must be surrounded by a number of servants before it can claim to be fully operational. Fig. 2.23 shows a typical microprocessor unit surrounded by some combination of peripherals.

2.8.2.1 Read-Only Memory (ROM)

Fig 2.23 shows a single ROM, there may be others. A ROM contains what is called the monitor or executor. The term executor is particularly apt, because therein are contained the microcomputer's operational orders in the form of various subroutines required for organising the system and ensuring proper operation. Examples of such subroutines are

1. address building;
2. interrupt sequencing;
3. memory examine and exchange;
4. power up sequence
5. code interpretation (e.g. operational instructions, provision for outputting etc)
6. peripheral interface adapter (PIA) input/output

The complete program for a dedicated computer would also be contained in ROM.

2.8.2.2 Random Access Memory (RAM)

The RAM is the "bank" that is used for temporary deposits and withdrawals of data or information required for the establishment of programmes. The programme itself may be held in either the ROM or the RAM. Should the programme require modification from time to time it would require random access, hence the RAM. In both the RAM and the ROM, data or operational instructions are held in the form of a single 8-bit byte.

2.8.2.3 Peripheral Interface Adapter (PIA)

The PIA provides one form of bridge between the computer and the outside. It handles data in parallel fashion in that all the 8-bit in each byte of information or data are processed simultaneously. It is obvious then why those eight separate lines into and out of the PIA are required.

Fig. 2.24 shows a simplified schematic diagram of typical Motorola 6820 PIA. The device provides two separate sections, each serving a primary 8-bit port. The in/out buses, designated A and B, with lines PA0 to PA7 and PB0 to PB7, are shown at the bottom side of the diagram. Each separate line in each port can be made to serve as single input or output line. Any combination of input/output may be added as required. For example:

1. lines PA0, PA1, and PA5 could be selected as input for receiving information from the outside the computer and the remaining lines used as output lines; or
2. all A-lines could be made output and all B-lines inputs; or
3. any other combinations could be used.

Software assignment of the basic line function is called configuring. At appropriate locations in the operating programme, the input/output line must be defined (Marrangoni, 1993; Segal et al., 1983).

2.8.2.4 Asynchronous Interface Adapter (ASCIA)

The ASCIA is a second type of connection, or bridge into and out of the computer. Whereas the PIA handles data in parallel form, the ASCIA does so serially. Serial transmission of digital information is generally used between such devices as a computer and keyboard, video display, printers, and the like. Serial handling is also used for long-line transmission, where cost of multiple parallel lines becomes prohibitive. Often a universal

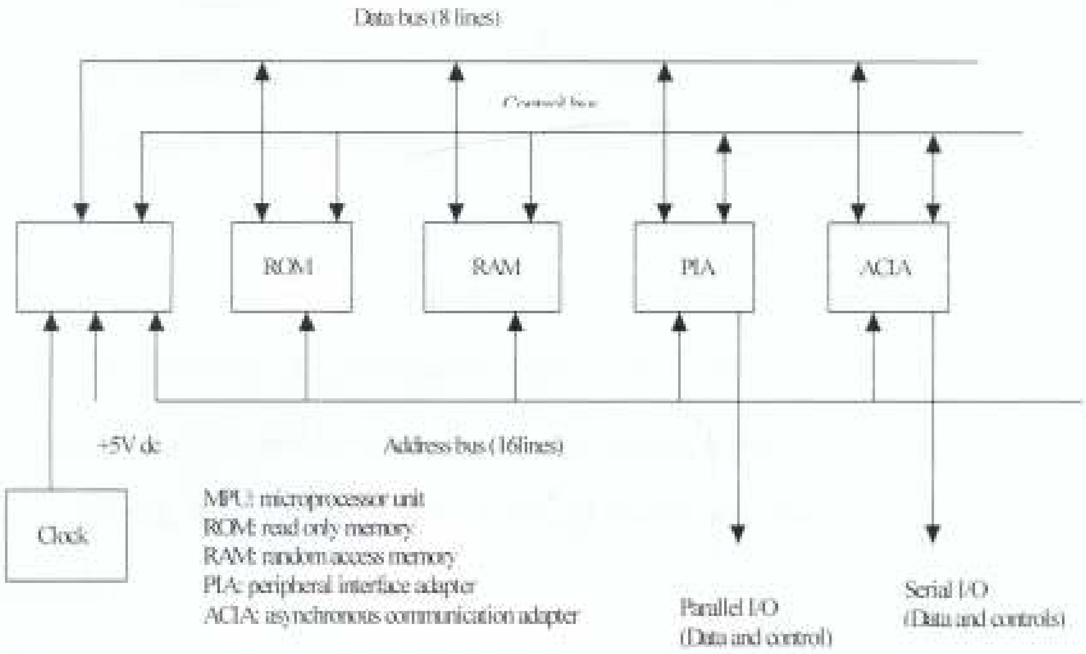


Fig.2.23: The microcomputer memory system layout

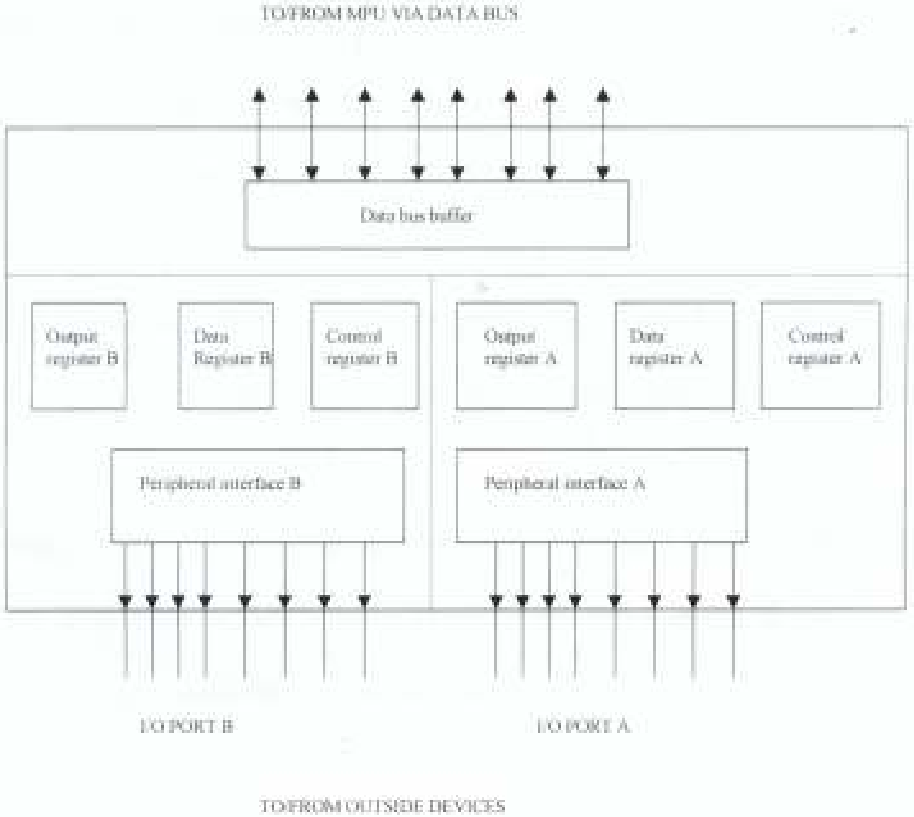


Fig.2.24 Simplified schematic diagram of a typical Motorola 6820 PIA

asynchronous receiver and transmitter (UART) is used to convert from the parallel format used by the computer to the serial format for output.

2.8.3 Analogue-to-Digital and Digital-to-Analogue Conversion

As discussed earlier in section 2.5.5 some measurements originate in digital form. Most mechanical inputs however exist in analogue form. Hence before digital data processing can be accomplished, an analogue-to-digital conversion is necessary. In like manner if a computer output is used to drive an analogue device, a digital-to-analogue conversion must be performed. Analogue-to-digital (A/D) and digital-to-analogue (D/A) conversion can be executed using a variety of circuits.

2.8.3.1 A Digital-to-Analogue Converter

A simple D/A converter is based on the summing amplifier. Referring to Fig 2.25 it is seen that the current summed is controlled by some digital switches. Four basic elements are involved, these are:

1. a stable reference voltage E_{ref}
2. a ladder arrangement of summing resistors. For this 8 bit word, eight summing resistors are used. The resistance values increase in a sequence of the power of two from R to 128R.
3. a series of switches that are solid state gates. The eight switches can be activated by TTL inputs, so their operation may be controlled by their respective bits, contained in a single byte of data.
4. Op-amp output circuitry. The op-amp output voltage is equal to $-R_f$ times the sum of the current from each ladder branch. The gain control resistor, R_f, is selected to scale the output voltage to a desire maximum value, 10V say.

When a switch is closed, a current is delivered to the inverting input of the op-amp in proportion to circuit resistor: switch 0 contributes i_0 = E_{ref} /128R, switch 1 contributes i_1 = E_{ref} /64R and so on.

Hence switch 0 corresponds to the least significant bit b_0, switch 7 corresponds to the most significant bit b_7; e.t.c. By closing selected switches the output voltage may be made proportional to any particular 8-bit number. Because of its increasing use in many digital applications, DAC now come in IC varying from 3-bit to as high as 16-bit converter. The ZN425 and DAC-08 are popular 8-bit digital-to-analogue converters in use today (Carr, 1987).

2.8.3.2 An Analogue-to Digital Converter

One typical circuit of the A/D converter is shown in Fig. 2.26. The circuit uses a set of voltage comparators and a series of resistors to simultaneously compare an analogue input signal with a set of reference voltages. The basic elements are as follows:

1. a stable reference voltage E_{ref}
2. a series of resistors; which form a voltage divider between E_{ref} and ground. For this 3-bit converter, eight resistors are used. The voltages at the nodes between resistors increase in steps of E_{ref} / 8
3. a set of voltage comparators: The analogue voltage is simultaneously compared with the voltage at each node. A comparator output is high when V_{in} is above the node voltage and low when it is below. Seven (2^3 -1) comparators are needed for the 3-bit converter.
4. an encoder circuit: the encoder reads the seven comparator outputs and produces a 3-bit binary output corresponding to one of the decimal number 0 to 7.

The digital output is shown as a function of V_{in}. The Fig 2.27 shows the Parallel A/D conversions form, they are particularly fast since all bits are set simultaneously, for which reason it is sometimes called flash encoding.

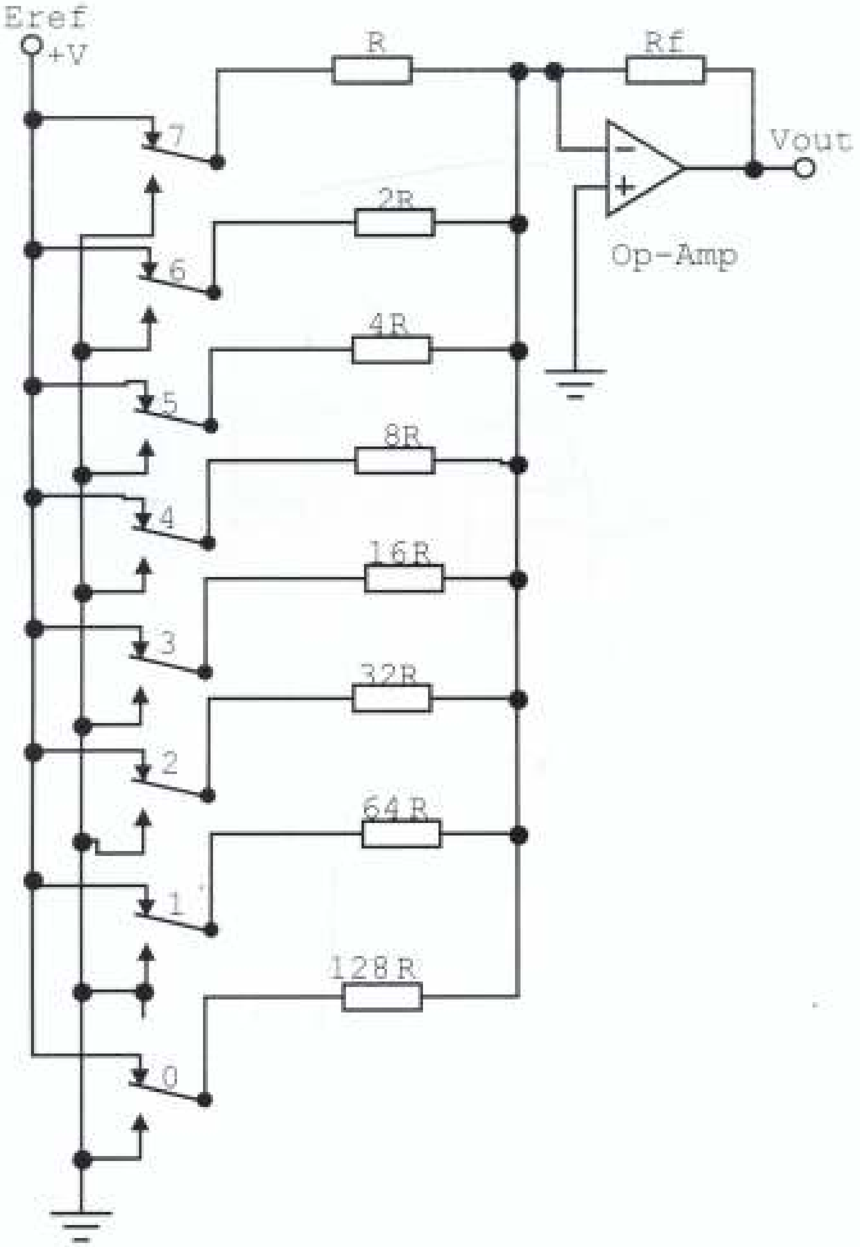


Fig.2.25: A simple 8-bit D\A converter

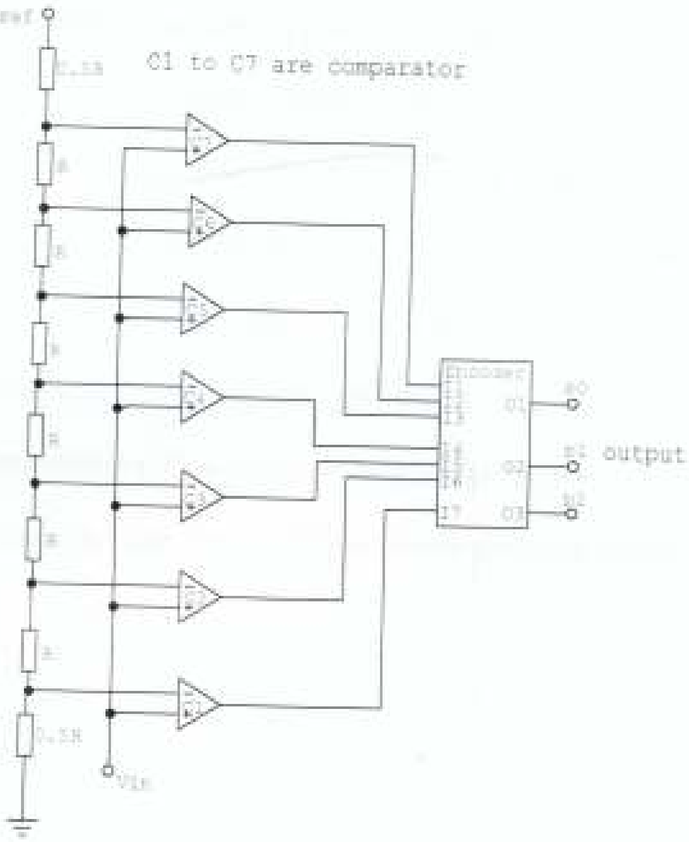


Fig.2.26: A 3-bit parallel A\D converter

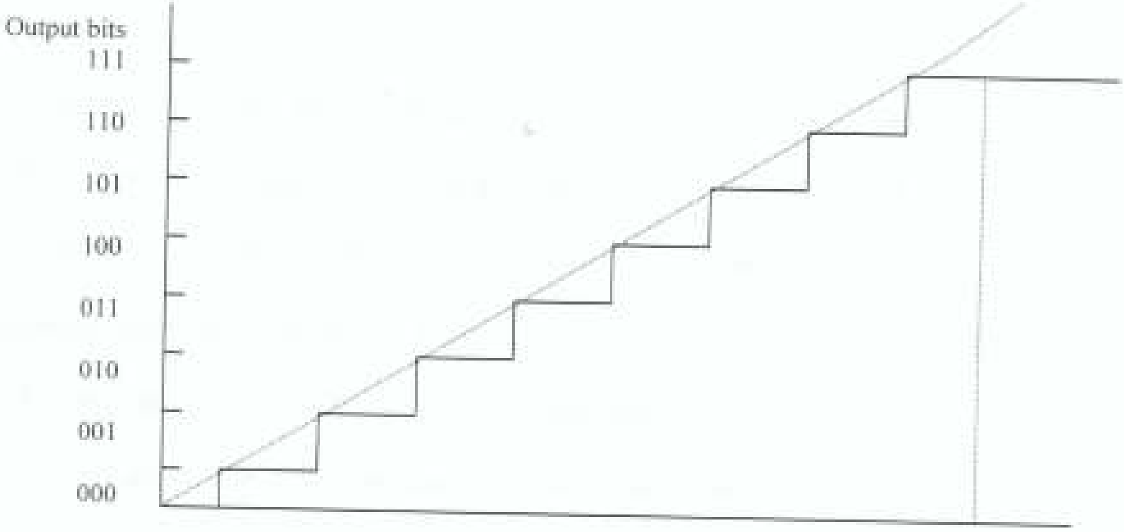


Fig.2.27: Digital output as a function of input analogue voltage to the ADC

2.8.3.3 Analogue-to-Digital Conversion Considerations.

Saturation Error: The most obvious limitation of an A/D converter is that it has defined upper and lower limits of voltage response. Typically full-scale ranges are 0 to 10V and -10V to +10V. If the input signal exceeds the upper or lower limit of response, the converter saturates and the recorded signal does not vary with the input. This situation can be prevented by appropriate signal conditioning, such as amplitude attenuation or dc offset removal.

Resolution and Quantization Error: An A/D converter responds to discrete changes in the input voltage. For example each step of a 3-bit converter corresponds to changes in V_{in} of Eref/8. Thus there is a minimum increment of voltage that can be resolved by the A/D converter. In general, the voltage resolution per bit, ε_v depends on the full-scale voltage and the number of bits of the converter:

$$\varepsilon_v = \frac{V_{fs}}{2^n} \tag{2.6}$$

Where V_{fs} is the full-scale voltage range

n is the number of bits of the A/D converter.

Typical A/D converters have 8, 12, 16 or more bits corresponding to division of V_{fs} into a total of 256, 4096, and 65536 increments.

The finite resolution of the A/D converter introduces error in the recorded values, since the actual analogue voltage usually lies between the available bits level. This is called quantization error, and it is entirely analogous to the reading error of a digital display. Using an A/D converter with more bits may reduce quantization error (Hall, 1989).

Conversion Error: An A/D converter may also suffer from non-linearity, zero offset error, scale error, or hysteresis. Such errors are a direct by-product of the particular method of input quantization. For example the conversion presented at Fig. 2.27 is on the average low by one-half of the least significant bit (the amount by which the solid curve lies beneath the dashed line). Normally the manufacturer will provide specification for the potential size of such conversion error.

Sample Rate: The rate at which an A/D converter records successive values of a time-varying input is called the sample rate. Each A/D converter has a maximum possible sample rate of which typical value ranges from about 1000Hz to more than 100MHz. Software often allows us to specify any sample rate up to this maximum value.

Signal Conditioning for A/D Conversion: To make the best use of an A/D converter, conditioning of the analogue signal is often required. The most important consideration is prevention of aliasing, minimization of quantization error, and prevention of saturation error. Aliasing can be prevented by using a low pass or antialiasing filter to remove frequencies of $f_{sample}/2$ or more from the analogue signal. Quantization error can be minimised by amplifying the signal to span as much as the full-scale range as possible. However this approach often conflicts with the need to avoid saturation error, so a compromise has to be reached.

2.9 INTERFACING THE STANDARD PARALLEL PORT

The Parallel Port is the most commonly used port for interfacing the computer to the outside world. This port allows the input of up to 9-bit or the output of 12-bit at any one given time; it is composed of 4 control lines, 5 status lines and 8 data lines. It is found commonly on the back of the personal computer as a D-type 25 Pin female connector. There may also be a D-type 25 pin male connector (Peacock, 2001)

Newer Parallel Ports are standardised under the IEEE 1284 standard first released in 1994. This standard defines 5 modes of operation, which are:

1. Compatibility Mode.
2. Nibble Mode
3. Byte Mode.
4. EPP Mode
5. ECP Mode

The aim is to design new drivers and devices, which are compatible with each other and also backward compatible with the Standard Parallel Port (SPP). Compatibility, Nibble and Byte modes use just the standard hardware available on the original Parallel Port cards while EPP and ECP modes require additional hardware which can run at faster speeds, while still being downwards compatible with the Standard Parallel Port.

Compatibility mode or "Centronics Mode" as it is commonly known can only send data in the forward direction at a typical speed of 50 kilo-bytes per second but can be as high as 150+ kilo-bytes per second. In order to receive data, one must change the mode to either Nibble or Byte mode. Nibble mode can input a nibble (4-bit) in the reverse direction. e.g. from device to computer. Byte mode uses the Parallel's bi-directional feature (found only on some cards) to input a byte (8-bit) of data in the reverse direction.

Extended and Enhanced Parallel Ports (EPP) use additional hardware to generate and manage "handshaking". This limits the speed at which the port can be run. The EPP & ECP ports get around this by letting the hardware check to see if the printer is busy and generates a strobe and appropriate handshaking. This means only one I/O instruction needs to be performed, thus increasing the speed. These ports can output at around 1-2 megabytes per second. The ECP port also has the advantage of using Direct Memory Access (DMA) channels and First In First Out (FIFO) buffers, thus data can be shifted around without using I/O instructions (Stewart, 2001)

2.9.1 HARDWARE REQUIREMENT

Table 2.2 shows the "Pin Outs" of the D-type 25-pin connector and the Centronics 36-pin connector. The D-type 25-pin connector is the most common connector found on the Parallel Port of the computer, while the Centronics connector is commonly found on printers. The IEEE 1284 standard however specifies 3 different connectors for use with the Parallel Port. The first one, 1284 Type A is the D-type 25 connector found on the back of most computers. The 2nd is the 1284 Type B, which is the 36 pin Centronics connector, found on most printers. IEEE 1284 Type C however, is a 36 conductor connector like the Centronics, but smaller. This connector is claimed to have a better clip latch and better electrical properties and it is easier to assemble. It also contains two more pins for signals, which can be used to see whether the other device connected has power. The 1284 type C connectors are recommended for new designs (Peacock, 2001).

Table.2.2 uses "n" in front of the signal name to denote that the signal is active low. E.g. nError. This line normally is high, should the printer be functioning correctly. If the printer makes an error then this line is low. The "Hardware Inverted" means that the signal is inverted by the Parallel card. Such an example is the Busy line. If Logic 1 (+5V) is applied

Table 2.2 Pin assignments of the D-type 25 pin parallel port connector.

Pin No (D- 25)	**Pin No Centronics**	**SPP Signal**	**Direction In/out**	**Register**	**Hardware Inverted**
1	1	nStrobe	In/Out	Control	Yes
2	2	Data 0	Out	Data	
3	3	Data 1	Out	Data	
4	4	Data 2	Out	Data	
5	5	Data 3	Out	Data	
6	6	Data 4	Out	Data	
7	7	Data 5	Out	Data	
8	8	Data 6	Out	Data	
9	9	Data 7	Out	Data	
10	10	nAck	In	Status	
11	11	Busy	In	Status	Yes
12	12	Paper-Out Paper-End	In	Status	
13	13	Select	In	Status	
14	14	nAuto-linefeed	In/Out	Control	Yes
15	32	nError nFault	In	Status	
16	31	nInitialize	In/Out	Control	
17	36	NSelect printer nSelect-In	In/Out	Control	Yes
18 - 25	19-30	Ground	Gnd		

to this pin and the status register read, it would return back a logic 0 in Bit 7 of the Status Register. The output of the Parallel Port is normally at TTL logic levels. Most Parallel Ports implemented in ASCIA, can sink and source around 12mA. These are just some of the figures taken from manufacturer Data sheets, Sink/Source 6mA, Source 12mA/Sink 20mA, Sink 16mA/Source 4mA, Sink/Source 12mA. (Anderson, 1996).

2.9.2 PARALLEL PORT ADDRESSING

The Parallel Port has three commonly used base addresses. These are listed in Table 2.3. The 3BCh base address was originally used for Parallel Ports on earlier Video Cards. They have now reappeared as an option for Parallel Ports integrated onto motherboards, upon which their configuration can be changed using Basic Input and Output System (BIOS). LPT1 is normally assigned base address 378_h, while LPT2 is assigned 278_h. However this may not always be the case as explained later. 378_h and 278_h have always been commonly used for Parallel Ports. The lower case h denotes that it is in hexadecimal. These addresses may change from machine to machine.

When the computer is first turned on, BIOS (Basic Input/Output System) determines the number of ports on the motherboard of a computer and assigns device labels LPT1, LPT2 and LPT3 to them. BIOS first looks at address $3BC_h$. If a Parallel Port is found here, it is assigned as LPT1, and then it searches at location 378_h. If a Parallel card is found there, it is assigned the next free device label. This would be LPT1 if a card was not found at $3BC_h$ or LPT2 if a card was found at $3BC_h$. The last port of call is 278_h and follows the same procedure as the other two ports. Therefore it is possible to have a LPT2 which is at 378_h and not at the expected address 278_h (Peacock, 2001).

Some manufacturers of Parallel Port Cards have jumpers that allow the Port to be configured as LPT1, LPT2, or LPT3. On the majority of cards LPT1 is 378_h, and

Table 2.3: Port Addresses

Address	**Notes:**
3BCh - 3BFh	Used for Parallel Ports which were incorporated on to Video Cards - Doesn't support ECP addresses
378h - 37Fh	Usual Address For LPT 1
278h - 27Fh	Usual Address For LPT 2

Table 2.4: LPT Addresses in the BIOS Data Area

Start Address	**Function**
0000:0408	LPT1's Base Address
0000:040A	LPT2's Base Address
0000:040C	LPT3's Base Address
0000:040E	LPT4's Base Address (Note 1)

LPT2, 278_h, but some use $3BC_h$ as LPT1, 378_h as LPT1 and 278_h as LPT2. The assigned devices LPT1, LPT2 and LPT3 should not be a worry for interfacing devices to PC's. Most of the time the base address is used to interface the port rather than LPT1 etc. When BIOS assigns addresses to a printer device, it stores the address at specific locations in memory, the address of LPT1 or any of the Line printer devices are on lookup table provided by BIOS which can be accessed at boot up of the computer. Table 2.4 is a typical BIOS address allocations for all LPT found on a given board.

2.9.3 SOFTWARE REGISTERS FOR THE STANDARD PARALLEL PORT (SPP)

If the Port is Bi-Directional then Read and Write Operations can be performed on the Data Register. The base address usually called the Data Port or Data Register is simply used for outputting data on the Parallel Port's data lines (Pins 2-9). This register is normally a write only port. Any read operation from the port will give back the last byte sent. However if the port is bi-directional, data could be received on this address. Table 2.5 gives the data port properties

The Status Port (base address + 1) with the properties shown in Table 2.6 is a read only port. Any data written to this port is often ignored. The Status Port is made up of 5 input lines (Pins 10,11,12,13 and 15), an IRQ status register and two reserved bits. It should be noted that Bit 7 (Busy) is an active low input. For example if bit 7 happens to show a logic 0, this means that there is a logic 1 (+5V) at pin 11. Likewise with Bit 2. (nIRQ) If this bit shows a '1' then an interrupt has not occurred.

The Control Port (base address + 2) with the properties shown in Table 2.7 is intended as a write only port. When a printer is attached to the Parallel Port, four "controls" are used. These are Strobe, Auto Linefeed, Initialise and Select Printer, all of which are inverted except Initialise. The printer does not send a signal to initialise the computer, nor does it tell the computer to use auto linefeed. However these four outputs can also be used for inputs. If the computer has placed a pin high and a device wants to take it low, one would effectively short out the port, causing a conflict on that pin. Therefore these lines are "open collector" outputs (or open drain for CMOS devices). This means that it has two states. A low state (0v) and a high impedance state (open circuit).

Normally the Printer Card has internal pull-up resistors, but as one would expect, not all will. Some may just have open collector outputs, while others may even have normal Totem pole outputs. In order to make our device work correctly on as many Printer Ports as possible, one can use an external resistor as well. Should one already have an internal resistor, then the two resistors act in parallel. If it is a Totem pole output, the resistors act as a load. An external 4.7kΩ resistor can be used to pull the pin high. If a resistor of lower value were used as the external resistor it would act in parallel giving effectively, a lower value of pull up resistor. When in high impedance state the pin on the Parallel Port is high. When in this state, the external device can pull the pin low and have the control port change to read a different value. In this way the 4 pins of the Control Port can be used for bi-directional data transfer. However the Control Port must be set to xxxx0100 for it to be able to read data that is all pins to be at logic 1 at the port so that you can pull it down to GND (logic 0) (Peacock, 2001).

Bits 4 and 5 are internal controls. Bit 4 enables the IRQ and Bit 5 enables the bi-directional port meaning that you can input 8 bits using (DATA 0-7). This mode is only possible if the computer card supports it. Bits 6 and 7 are reserved. Any write to these two bits will be ignored.

Table 2.5: Data Port

Offset	**Name**	**Read/Write**	**Bit No.**	**Properties**
Base + 0	Data Port	Write (Note-1)	Bit 7	Data 7
			Bit 6	Data 6
			Bit 5	Data 5
			Bit 4	Data 4
			Bit 3	Data 3
			Bit 2	Data 2
			Bit 1	Data 1
			Bit 0	Data 0

Table 2.6: Status Port

Offset	**Name**	**Read/Write**	**Bit No.**	**Properties**
Base + 1	Status Port	Read Only	Bit 7	Busy
			Bit 6	Ack
			Bit 5	Paper Out
			Bit 4	Select In
			Bit 3	Error
			Bit 2	IRQ (Not)
			Bit 1	Reserved
			Bit 0	Reserved

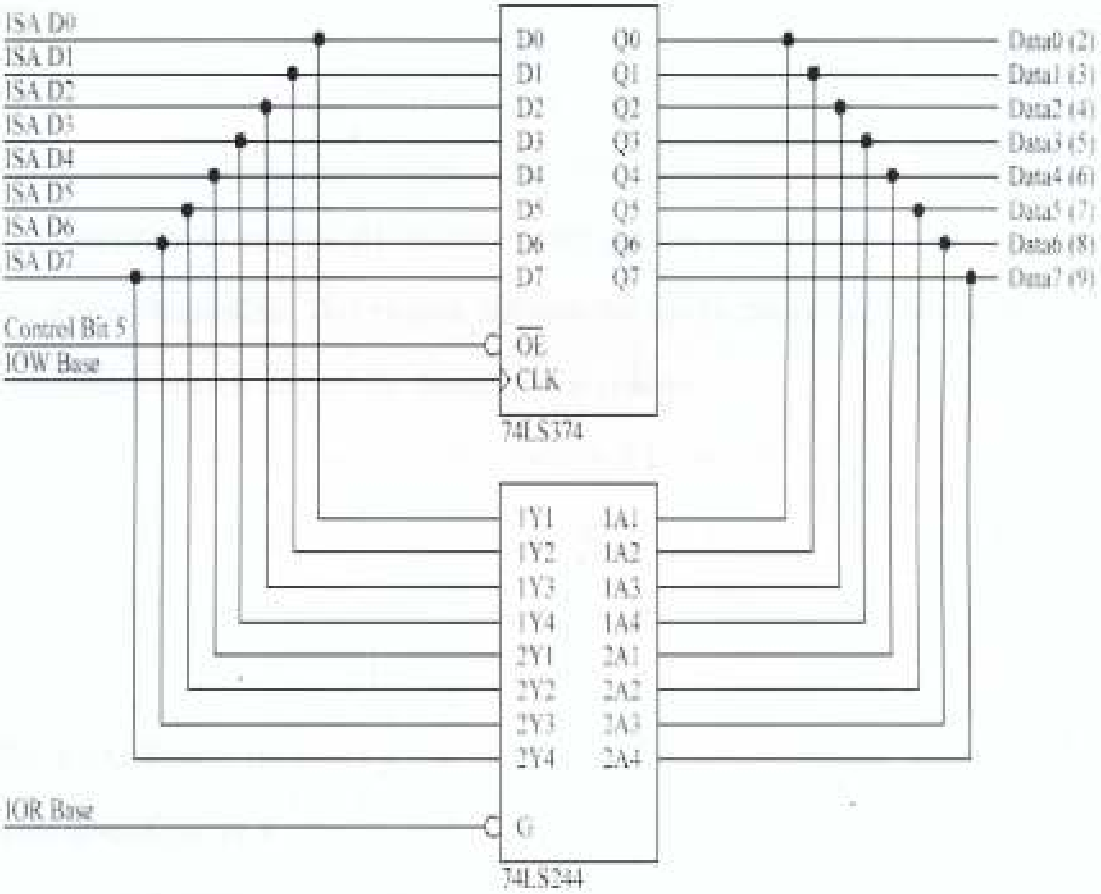
Table 2.7: Control Port

Offset	**Name**	**Read/Write**	**Bit No.**	**Properties**
Base + 2	Control Port	Read/Write	Bit 7	Unused
			Bit 6	Unused
			Bit 5	Enable Bi-directional Port
			Bit 4	Enable IRQ Via Ack Line
			Bit 3	Select Printer
			Bit 2	Initialize Printer (Reset)
			Bit 1	Auto Linefeed
			Bit 0	Strobe

2.9.4 BI-DIRECTIONAL PORT MODE

The schematic diagram shown in Fig. 2.28 is a simplified view of the Parallel Port's Data Register. The original Parallel Port cards implemented 74LS logic. Nowadays all this is crammed into one ASIC, but the theory of operation remains the same. The non bi-directional ports were manufactured with the 74LS374's output enable tied permanently low, thus the data port is always output only. When a read operation is performed on the Parallel Port's data register, the data comes from the 74LS374 which is also connected to the data pins. Now if one can overdrive the 374 it can be effectively turned into a Bi-directional Port. (Or an input only port, once the latch outputs has been blown up!)

Bi-directional ports use Control Bit 5 connected to the 374's Output Enable so that its output drivers can be turned off. This way one can read data present on the Parallel Port's Data Pins, without having bus conflicts and excessive current drains. Bit 5 of the Control Port enables or disables the bi-directional function of the Parallel Port. This is only available on true bi-directional ports. When this bit is set to one, pins 2 to 9 go into high impedance state. Once in this state one can enter data on these lines and retrieve it from the Data Port (base address). Any data written to the data port is stored but it is not available at the data pins. To turn off the bi-directional mode, bit 5 of the Control Port is set to '0'. However not all ports behave in the same way. Different manufacturers implement their bi-directional ports in different ways.



Standard Parallel Port Bi-Directional Operation

Fig.2.28: Standard parallel port Bi-directional operation

CHAPTER THREE

DESIGN AND DEVELOPMENT OF A PRECISION THERMOMETRIC SYSTEM

3.1 INTRODUCTION

Precision temperature measurement to a large extent depends on the stability and precision of the monitoring device. Since most of the system design is basically electronics, it becomes imperative to employ all the knowledge acquired from chapter two on precision design and error budgeting. This chapter presents the design parameters used in the design and development of each stage of the thermometric system.

To fully describe the entire circuitry used in the accomplishment of this project, it is divided it into two major parts (a) The Analogue and (b) The Digital Design part. The latter consists of (i) the digital circuit design and (ii) software design

3.2 THE ANALOGUE DESIGN REQUIREMENT

3.2.1 THERMOCOUPLE

The choice of a thermocouple for temperature measurement is usually dependent on three major factors;

(a) the range of temperature to be measured.

(b) the environmental condition in which the measurement is to be taken.

(c) the degree of accuracy, consistency and sensitivity required for repeated measurement operation using the same thermocouple (Perrin, 1999 , 2000).

Thermocouples are given a letter designation that indicates the material they are fabricated from. This letter designation called thermocouple type, classify commonly available standard thermocouples into their usable temperature ranges (Labfacility, 2001).

Each thermocouple type produces a different open circuit voltage for a given set of temperature conditions. None of these devices is linear over a full range of temperature (Perrin, 1999). Therefore standard tables are available that tabulate Seebeck voltage as a function of temperature. Also there is a standard polynomial model available for each thermocouple (Labfacility, 2001).

In many applications the range of temperature being measured is sufficiently small that the Seebeck voltage is assumed to be linear over the range of interest. This eliminates the need for look up tables or polynomial computation in the system. However for the purpose of this application which covers a temperature range from 50°C to 1500°C and for reason of the deteriorating effect which the environment of the furnace could have on the thermocouple, the thermocouple of choice is the type S which is made of Platinum Rhodium versus platinum.

From the standard table for this thermocouple it has a lower limit at 0°C given a Seebeck voltage output of zero emf with the reference junction fixed at the triple point of water i.e 0°C and an upper limit of 1700°C with an output e.m.f. of 18.59mV. Appendix A gives the temperature and corresponding output voltage of a standard S type thermocouple. This is based on the international temperature scale of 1948 with reference junction at 0°C. For accuracy all measured output voltages are normally referenced to the standard chart containing a curve of temperature versus voltage for the thermocouple type.

Table 3.1: Shows the commercially available standard thermocouple

TYPE	MATERIALS		USABLE TEMPERATURE RANGE IN °C
B	Positive Side Pt + 30% Rh	Negative Side Pt + 6% Rh	0 to 1820
E	Ni + 10% Cr (Nichrome)	Cu +43% Ni (Constantan)	-270 to 1000
J	Fe (Iron)	Cu + 43% Ni (Constantan)	-210 to 1200
K	Ni + 10%Cr (Nichrome)	Ni + 2% AL + 2% Mn + 1% Si (Alumel)	-27 to 1372
N	Ni + 14% cr + 1.5% Si (Nicrosil)	Ni + 4.5% Si + 0.1% Mg (Nisi)	-270 to 1300
R	Pt + 13% Rh	Pt	-50 to 1768
S	Pt + 10% Rh	Pt	-50 to 1768
T	Copper	Cu + 43% Ni (Constantan)	-270 to 400

3.2.2 THERMOCOUPLE AMPLIFIER

In the design of a thermocouple amplifier the following points were considered.

- The type of thermocouple to be used.
- The full range of temperature the hot junction will be exposed to.
- The full range of temperature the cold junction will be exposed to.
- The temperature resolution required for the application.
- Whether or not the system requires galvanic isolation
- The type of cold junction compensation required.

The sensitivity of thermocouple's output voltage is in the range of a few microvolts per degree change in temperature. To prevent the useful signal from being marred by noise that could be several milli-volts, in the design of the thermocouple amplifier, attention was focussed on noise rejection and common mode error rejection.

Many integrated circuit modules are advertised in catalogues, which meet some of the requirements listed. Such modules are expensive and not readily available. Therefore it became desirable to build a workable circuit from readily available parts such as op-amps and other discrete components. As described in chapter two on error budgeting, a well designed thermocouple amplifier takes into consideration the following requirements.

(a) the amplifier circuit should present high input impedance to the transducer so as to limit the error due to self-heating in the thermocouple.

(b) the op-amp should be one with low input bias current, low output offset voltage, small thermal drift, high CMRR and high power supply rejection ratio (PSRR). The op-amp should have provision for offset nulling.

(c) discrete components such as capacitors and resistors were those with low temperature coefficient, since the amplifier circuit is to be mounted in an area of ambient temperature close to 40°C.

3.2.3 VOLTAGE-TO-FREQUENCY/ FREQUENCY-TO-VOLTAGE CONVERTERS

The voltage-to-frequency converter (V/F) finds wide application in measurement systems where transmission of signals is over a relatively long distance and through cable, radio or optical fibre. The mode of signal transmission depends on the application at hand. For this work FM TELEMETRY is used and basically it involves the use of radio signals transmission.

The output signal in d.c. voltage from the thermocouple amplifier is converted to a time dependent varying signal that is proportional to the input voltage. Voltage-to-frequency converters can easily be assembled from discrete components and trimmed to meet the required linearity. Because of the rapidly increasing need of these converters in system design, manufacturers have come out with such converters in IC form. This is available as single chip in market with varying degree of linearity and drift, among the common types available are the LM331, AD537, VFC 32, TSC 9400-02 and the RC 4151 & 4152 (Franco, 1988).

For this work, the LM331 is used extensively. It is a simple V/F converter suitable for use in analogue-to-digital conversion, precision F/V conversion and many other applications. Fig 3.1 shows the IC pin-out. When the IC is used as a voltage-to-frequency converter, it produces a pulse train, which is linearly proportional to the applied input voltage. The device uses a temperature compensated band-gap reference circuit to provide very good accuracy over the entire operating temperature range. Although the precision timer circuit has a low bias current, the response is sufficiently fast for 100 kHz voltage-to-frequency conversions (low bias current often results in reduced switching speeds and restricted operating frequencies). The output of the device is capable of driving loads of between 5V (i.e. TTL level) and 40V, depending on the supply voltage, and is fully protected against short circuits to Vcc. Appendix B is a complete application note for LM331 from National Semiconductors

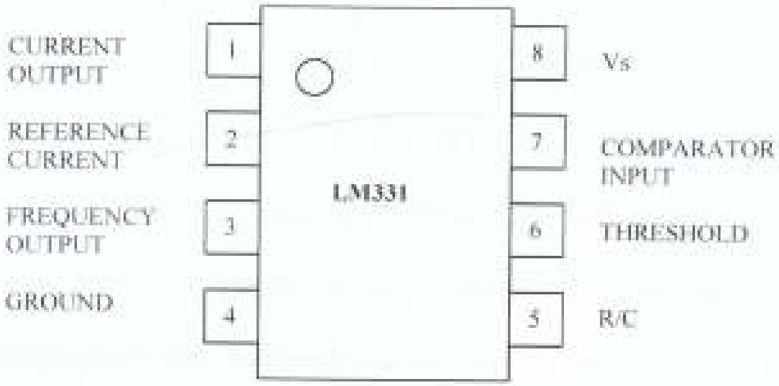


Fig.3.1: IC pin-out for the LM331 V\F and F\V converter

3.2.4 FM TRANSMITTER

The FM mode of radio transmission is widely adapted in radio telemetry because of its numerous advantages over other known means of radio signal transmission basically because of its immunity to noise and high penetrating power. Apart from this, FM receivers can be fitted with amplitude limiter to remove amplitude variation caused by noise. It is possible to reduce noise still further by increasing the modulation deviation angle since percentage modulation in excess of 100% is possible in FM without causing much distortion (Kenedy and Davis 1992). For this work the quality of useful signal received is not expected to suffer much distortion since they are pulses that can easily be reshaped. FM broadcast is also possible in the upper VHF and UHF Frequency range. Various methods of generation of frequency modulation is described in various communication texts (e.g. Kenedy and Davis, 1992)

3.2.5 ANALOGUE CIRCUIT DESCRIPTION

The circuit can be conveniently divided into two parts, the transmitter and receiver module. Fig. 3.2 shows the circuit diagram of the transmitter module. The thermocouple is a type 'S' which is adequate for the continuous measurement of temperature in the desired range of 50-1500°C. Its reproducibility of temperature measurement and ability to operate in both oxidising and reducing atmospheres make it an ideal choice (Perrin, 1999).

The thermocouple amplifier is built around *U1* a commercially available precision bi-polar op-amp (type OP-07). According to its manufacturer (National Semiconductor, 1994), the op-amp exhibits low drift with time and temperature (0.6mV/°C) and a low offset voltage (7.5mV max). The op-amp *U1* is operated in the non-inverting mode so that it presents a high input impedance to the thermocouple, a condition necessary for the proper operation of active transducers with low output impedance (Garrett, 1981).

The voltage gain of the amplifier is equal to *(RV2 + R7 +R6)/R6*. The gain is trimmed to 100 by adjusting the potentiometer *RV2* on Fig.3.2

The diode *D1* is in thermal contact with the thermocouple's cold junction and provides the means for the cold-junction compensation. At room temperature, the voltage drop across the diode *D1* is approximately 600mV. The potential divider formed by the resistors *R4* and *R5* makes the temperature coefficient of the voltage drop across the PN junction of the diode *D1* match the thermocouple sensitivity at 25°C which is approximately 0.14mV for type 'S'. This puts the potential at the inverting input of the op-amp of Fig.3.2 equal to 0.14mV.

As the ambient temperature increases above 25°C, the temperature coefficient of the diode voltage drops almost linearly with the rise in temperature (-2mV/°C for silicon diodes) (Franco, 1988). The cold junction compensation mismatch can be reduced to a sufficiently low level by trimming *R5* so that $\tau V_{BE}\ X\ R5/(R4 + R5)$, where τV_{BE} is the temperature coefficient of V_{BE} of *D1*, exactly matches the thermocouple sensitivity (Isaac et al., 1993). This results in a drop of –5.8μV/°C across the resistor *R5* acting as the reference point for the non-inverting input of U1 and this corresponds to a change close to the sensitivity of the thermocouple around ambient. This shows that the combination of diode *D1* and the resistors *R4* and *R5* adequately provides the required cold-junction compensation for the thermocouple. It is important to note that this scheme works only at a temperature above or around ambient.

U1 has provision for offset nulling on pins 1 and 8 and this is used to bring the output voltage of the thermocouple amplifier to zero for an initial zero input voltage, thus nulling the effect of the input offset voltage and in effect allowing for the operation of the amplifier with minimal drift. The potentiometer *RV1* is used for adjusting the output of the thermocouple amplifier to a required voltage value for known temperature at the thermocouples hot junction. This is done by inserting the thermocouple into a fixed temperature bath at 150°C and the thermocouple amplifiers output voltage trimmed to 103mV which corresponds to the expected thermocouple output emf X 100.

Diodes *D2* and *D3* protects U_1 inputs from damage that could result from transient upsurge voltage which may follow a thermocouple break or electrostatic discharge. The output of the thermocouple amplifier is fed to a voltage-to-frequency converter formed by the V/F LM331 and its associated components. The voltage on pin 7 and the values of resistors *R11 R10, R13 + RV3* and capacitor *C7* determine the frequency of the pulse output at any time. According to (Maplin, 2001), f is given by:

$$f = 0.486\frac{R13 + RV3}{R10.R11.C7}V_{in}\frac{kHz}{V}, \tag{3.1}$$

The output pulse height is determined by the value of the voltage to which *R12* is tied. It is worthy to note that the choice of resistive and capacitive components for the V/F converter is very critical, for values used in the implementation of this device linearity error was only about 1% as specified in the manufacturer design note (Maplin, 2001). The V/F converters output frequency per unit input voltage is adjusted by the 4.7kΩ trimmer resistor *RV3*. It was trimmed to give an output of 1Hz/mV. For a thermocouple amplifier output voltage of 30mV to 1555mV that corresponds to a temperature of 50°C—1500°C, the converter is expected to give an output pulse of frequency 30Hz to 1553Hz.

The output pulse is attenuated by a resistor combination of *R14* and *R15* with *R15* being trimmable to allow for adjusting the level of the input pulse needed for best modulation of the carrier wave.

The oscillator section of the transmitter is built around *T1* of Fig.3.2. Oscillation frequency is determined by the value of *L1, VC1* and *C10*, which forms the oscillating tank, for small value of *C10* the centre frequency can be approximated by the relation:

$$f = \frac{1}{2\pi\sqrt{LVC1}} \tag{3.2}$$

VC1 is used to set the centre frequency for best reception on the VHF receiver. *C10* is used as a feedback capacitor and it is usually in the range 1 to 5pf so that it as little effect on the centre frequency. This is required to sustain oscillation. Modulation is directly applied to the base of *T1* via *C8*. The transistor *T2* is a buffer that is used to drive a RF amplifier built around *T3* operating best at a frequency determined by *L2* and *C14*. The values for the components shown on Fig 3.2 are for maximum RF amplification. The signal is finally radiated as electromagnetic wave from the body of a 1mm thick, 50mm long copper wire, which act as the transmitting antenna.

The schematic diagram shown in Fig. 3.3 is the receiver module. It begins with a VHF receiver used to demodulate the transmitted pulses from the first module. The audio frequency output from the receiver is shaped to a square wave of amplitude 5V by the two CMOS inverters and its associated components, with *D4* and *D5* acts as a voltage limiter to keep the output from the receiver to a tolerable limit.

The square wave serves as input to a frequency to voltage converter built around another LM331 IC now configured as a F/V converter. The choice of components is such as to give a conversion factor of 1mV/Hz. for values of components shown the converter as a full-scale output voltage from 0 to 4V for input frequency 0 to 4 kHz. For input frequency 30Hz to 1553Hz the output voltage of the LM331 was trimmed for a voltage output of 50mV to 1553mV. The output from this converter stage is then buffered by the voltage follower U2, whose output is then attenuated and conditioned by resistor *R32* and capacitor *C20*. It is this voltage that serves as input to the next stage that is the digital conversion stage.

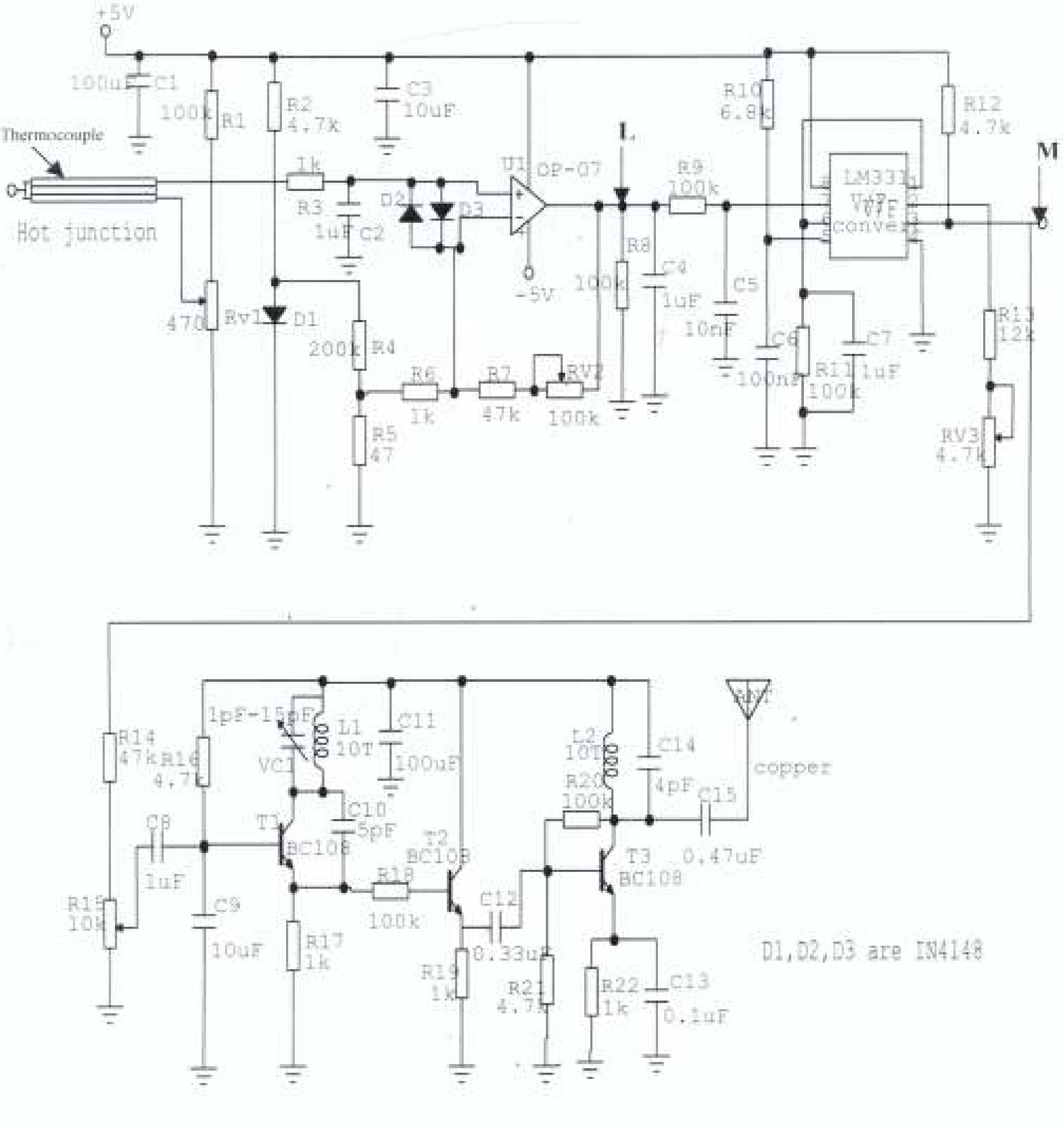


Fig.3.2: The telemetry transmitter circuit

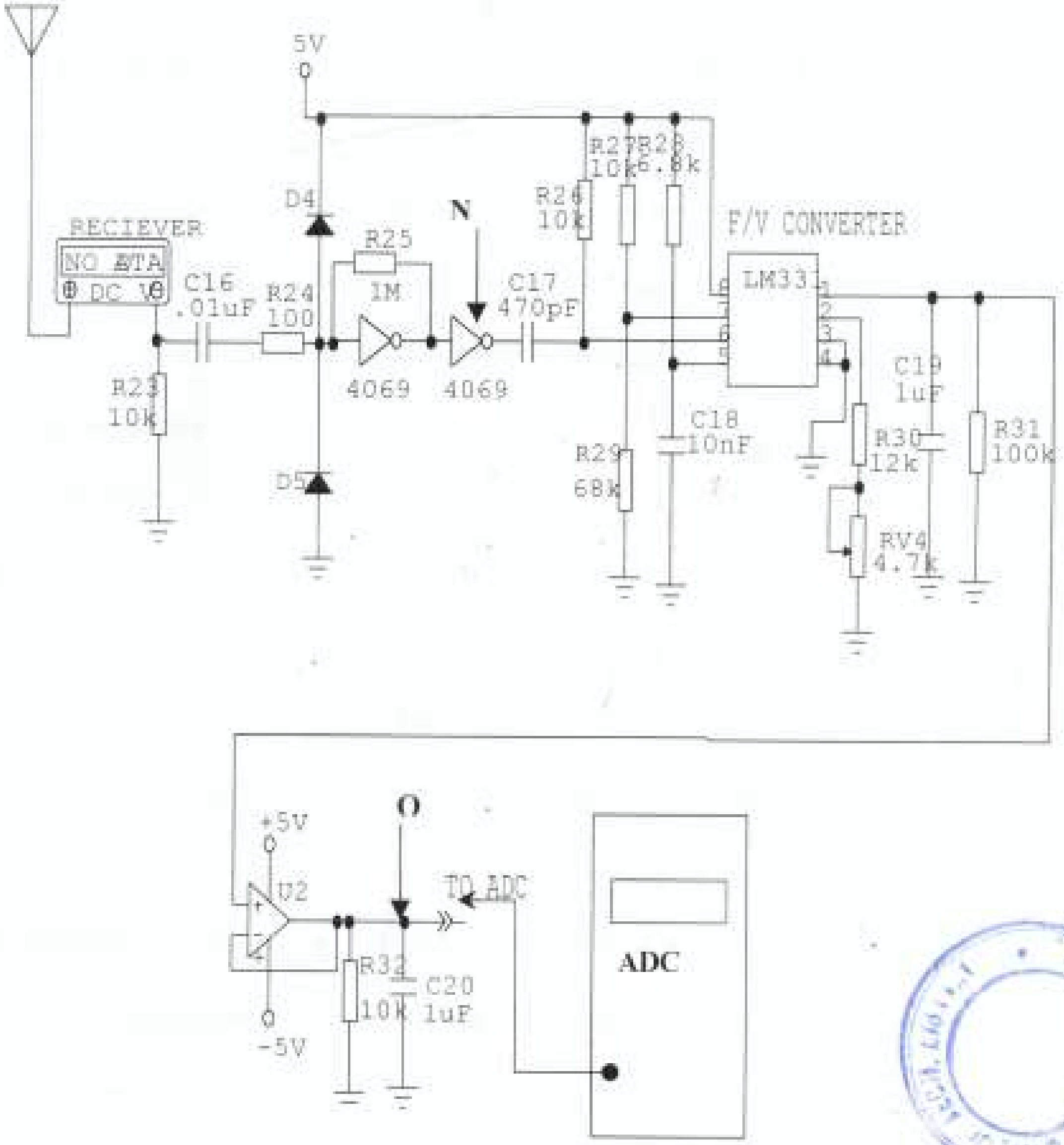


Fig.3.3: The radio telemetry receiver/converter circuit

3.2.6 DIGITAL INTERFACING CONSIDERATION

For this project the printer's port of the IBM compatible P.C. was adapted. This port is an inexpensive and yet powerful platform for implementation of project dealing with the control of real world peripherals. Fig 3.4 shows what the port looks like at the back of a personal computer desktop. The port provides eight TTL outputs D0- D7, five inputs S3-S7 and four bi-directional leads C0- C3. It provides a very simple means to use the PC interrupts structure.

An explicit discussion on the adaptation of the printers' port is a large manual on its own. Manuals that deal with the use of the printers' port for controls and data acquisition are available in text and on the Internet (http://www.access.digex.net/pha). Five modes exist for parallel interfacing as was described in section (2.9) earlier. For this work, the byte mode which allows the input and output of 8-bit at a time was adapted.

The TC7109 a 12-bit analogue-to-digital converter, a product of Microchip, used for the implementation of the digital module offers the following important features.

- Zero-integrator cycle for fast recovery from input overloads,
- Eliminates cross–talk in multiplexed systems,
- 12 bit plus sign integrating A/D converter with over-range indicator
- Low noise (-15 μVp-p typical)
- No Zero Adjustment needed
- TTL compatible, Byte-organised Tri-state outputs

The general description and application note for this device is presented in Appendix D.

Since the analogue-to-digital converter used is a 12-bit microprocessor (μP) compatible type to input this twelve bit using the same 8 bit port requires taking the information in a succession of 8 lower bits followed by the next 4 upper bits. The process of achieving this and the control of the interfacing network lie entirely on the driver software.

The programme is written in QBasic and also visual basic. The entire circuit layout for the interfacing and control software is presented next.

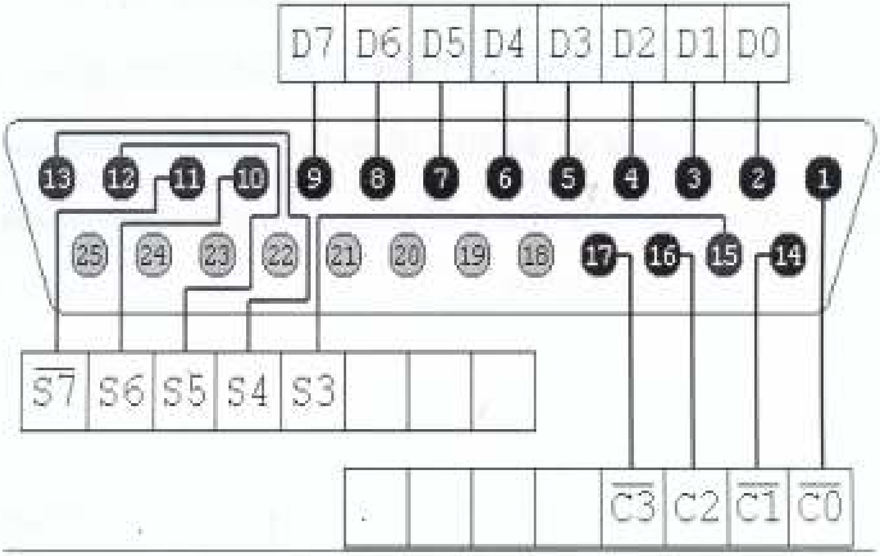


Fig.3.4: DB-25 printers port connection

3.2.6.1 DIGITAL CIRCUIT DESCRIPTION

The circuitry is conveniently divided into two modular parts, the A/D converter module and the interfacing adapter module. Fig.3.5 shows the entire module. It consists of a 12-bit A/D converter, two 4069 hex inverters and 12 LEDs as visual indicator for ease of calibration. The converter was set in a continuous conversion mode by tying pin 26 the RUN/HOLD to a high (+5V). Pins 18 through 21 set the operation of the converter for direct output mode and enabling both lower byte B1—B8 and the higher byte B9—B12, and also the polarity and over-range indicator outputs. The conversion rate was set to 30 conversions per second by the choice of *C4* and *R6* that form an RC oscillator for the system. To give a better rejection of line which result in an error of less than 1% from two 60 Hz periods or 33.33 millisecond.

A resolution of 1bit/mV was achieved by adjusting the reference-input voltage at pin 36. The combination of the zener diode *ZD1* and the potentiometer *VR1* allows for the trimming of the reference input voltage. This allows for a full-scale 12-bit output i.e. all outputs bits B1—B12 are high when an input voltage of 4096mV is placed at the input. The outputs B1—B12 serve as inputs to 12 inverters contain in the two 4069 CMOS IC. The inverter in turn drives 12 LEDs that serve as visual indicator signifying the state of each bit B1—B12.

The interfacing adapter consisting of two 74LS373 octal D-type latches, busses for connectivity and signal transmission and a D-25 male parallel port adapter. The outputs B1 to B12 from the A/D converter also serve as inputs for the 2 Octal latches, with B1—B8 as input to IC2 and B9—B12 as input to IC1. IC1 has 4 open inputs pin 13, 14, 17, and 18, which for safety against damage that could result from electrostatic charges are all grounded (Bernard .et al., 1977).

The busses carrying the output bit from the latches were crossed such that the 12 bit data under software control can be read in a succession of 8 bits followed by the other 4 bits. Most computers parallel port card outputs are designed as open collectors to enable compatibility with varying attached devices. To prevent excessive current drain, which could cause a permanent damage, the port output pins are tied to a high (+5V) through a 10kΩ resistor as shown in the Fig.3.5.

The control input pins 1 and 14 of the D-25 parallel port adapter are both active low i.e. a high placed on these pins by the computer processor is internally inverted. This is taken care of in the design of the control software. The output of the control pin 1 is connected to pins 11 the chip-enable of both octal latches. When a high is placed on this pin the output of both latches follows the ADC's 12 bits and when set low the outputs are latched. The control pin 14 is connected directly to pin 1 of IC2 and inverted by a CMOS inverter connected to pin 1 of IC1. This ensures that data are presented to the data port pins 2 through 9 of the D-25 adapter in an alternate pattern.

When the control pin 14 is set to a low, IC2 is enabled and its output are active while the output of IC1 are all set to high impedance caused by the inversion of the control bit to its pin 1. When this control bit is high the action is in the reverse with IC1's output being active and available through the busses to the data port. Tying the output as shown in Fig 3.5 is to achieve the said goals of inputting 12-bit of data through the 8-bit port available for byte mode transfer of data.

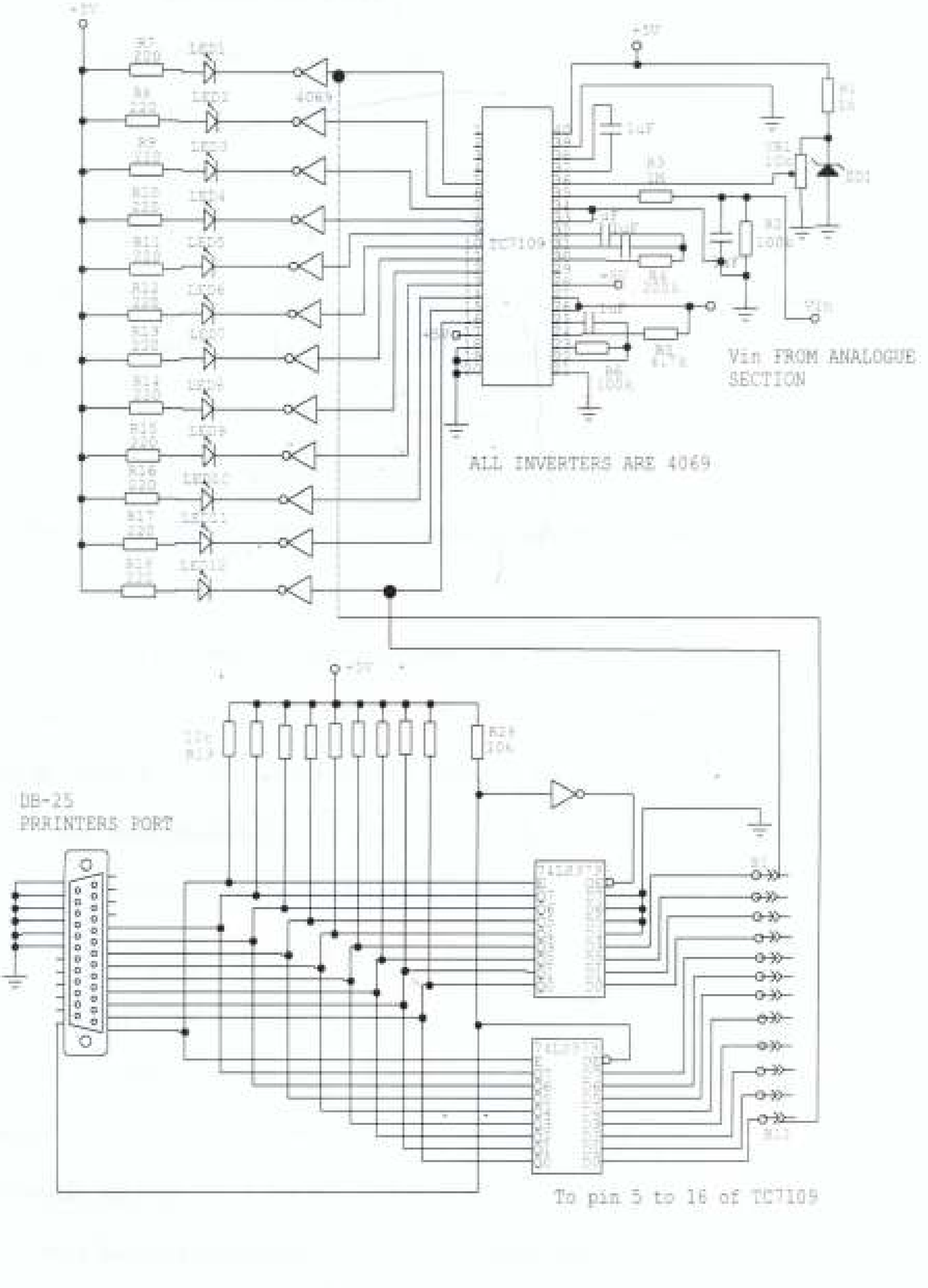


Fig.3.5: Circuit diagram of the analogue-to-digital converter and the interfacing adapter

3.2.6.2 SOFTWARE DESCRIPTION

The entire process of control, data read operation and further processing of the acquired data are all carried out by the computer software. The software programme was written in QBasic, which is a text mode program, and Visual Basic a window based programme. This program is then compiled as a stand alone executable programme to enable portability, compatibility to other systems and importantly to prevent the program from being corrupted and finally to increase the speed of operation (Nameroff, 1998).

The entire programme is made up of five sub-programs as demonstrated in the flow chart in Fig 3.6. First a graphical screen is prepared for inputs from the user and output of processed data. A file is then opened for both read and write for storage of data and a timer is initiated.

The main program then calls the control sub-program a DLL (Dynamic Link Library) which enables the programme control to interact with the external circuitry (Maver,1998). Data are read to a temporary memory location on the RAM of the computer. The manipulation and processing of the data is also carried out in the RAM, the result of which comes out as displayed on the graphical screen and at the same time stored in a permanent file at a time interval as provided by the user. Fig.'s 3.7 to 3.10 shows how the graphical screens for control and data logging look like. Fig 3.7 is a flash form that displays the product copyright ID. Fig 3.8 is the main control panel from where one can decide whether to recalibrate the ADC or proceed with the main operation of measuring and data logging temperature readings. Fig 3.9 is the recalibration form that recalibrates the ADC and produce a correcting factor by comparing a known input voltage into the ADC and the actual retrieved by the computer from the ADC . Fig 3.10 is the main operation form that displayed the measured temperature, time and date. It also has provision for selecting a drive and creating a sub-directory for which data logging is desired. It also has a means for setting the rate at

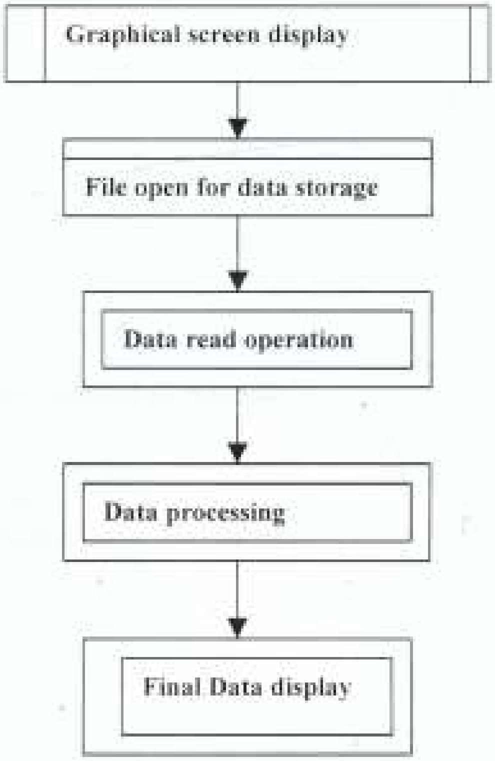


Fig.3.6: Flow chart of the software developed

which data could be logged. The time interval ranges from 1 second to 24 hours. It also has a provision for selecting the thermocouple type for use with the system .The button named caller is a provision that allows the user to adapt the system to suit other applications.

The following sub programme demonstrates how the data read operation is carried out.

3.2.6.2.1 Module for the control of the ADC

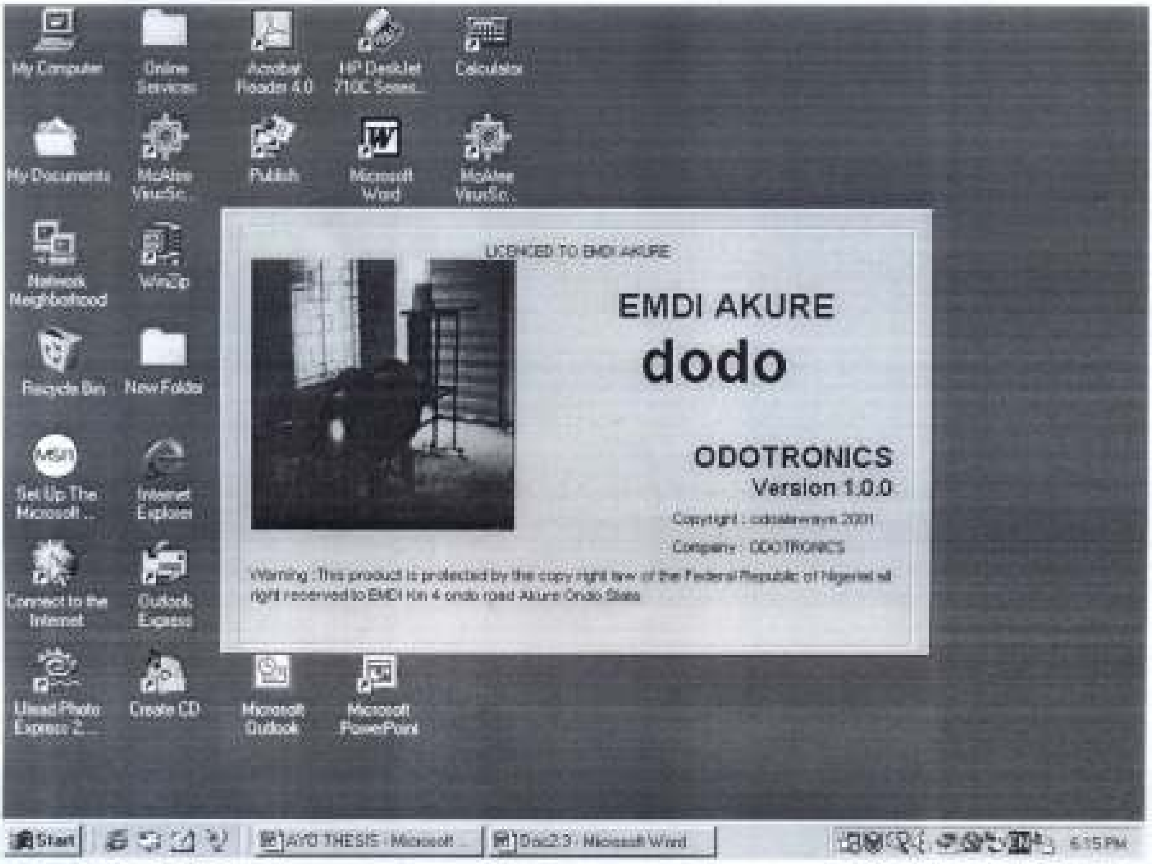
Line

```
1.  Option Explicit
2.  Public Function ADC() As Integer
3.  Dim first As Integer
4.  Dim second As Integer
5.  Dim result As Single
6.  Dim foward As Integer
7.  Dim fad(5) As Integer, rel As Integer
8. Dim E As Integer, N As Integer, S As Integer, p As Integer
9.  Rem READ OPERATION
10. Do While first = 0
11. Out 890, 252
12. For E = 1 To 200: Next E
13. Out 890, 255
14. For E = 1 To 200: Next E
15. first = Inp(888)
16. Loop
17. Let S = 0
18. Do
19.     Out 890, 253
20.     For E = 1 To 200: Next E
21.     second = Inp(888)
22.     S = S + 1
23.     If S = 200 Then
24.     p = 0
25.     Exit Do
26.     End If
27.      Loop While second = 0
28.     Select Case second
29.             Case 1: p = 256
30.             Case 2: p = 512
31.             Case 3: p = 768
32.             Case 4: p = 1025
33.             Case 5: p = 1280
34.             Case 6: p = 1536
35.             Case 7: p = 1792
36.             Case Else: p = 0
37.     End Select
```

```
38.     ADC = first + p
39.      End Function
```

Line 1 ensures that no undeclared variable is used. Line 2 declares the function ADC() a public integer so that it can be used by other sub programmes outside the main window. Lines 3 to 8 declare all the variable type used in the programme. Line 10 starts the read operation by initiating a loop. Line 11 outputs to the control port with port address 890 in decimal the code represented in decimal by 252 which initialises the 12-bit ADC card. Line 12 is a delay that allows the ADC enough time to fully respond to the control bits. Line 13 sends the code 255 to the control port to set the data port for bi-directional data transfer and at the same time connecting the 8 lower bits of the ADCs output to the data port. Line 14 is again a delay while line 15 is a command to read the 8-bit available at the data port and assigned the value read to the variable first. Line 16 checks the condition stated at line 10 and ensures that a none zero value is read, if a zero is read the operation is repeated. Line 18 through 27 is another loop operation that connects the remaining 4 higher bits to the data port, a counter is initiated that allows this value to be read for up to 200 times in the case the 4-bit is a zero, if it is non zero the loop is terminated on the first read operation and the final value read is assigned to the variable second. Line 28 to 37 is a comparison chart for the variable 'second' for the entire operation range seven levels at most is expected. If the value in the variable second is 1 then P is assigned 256 and so on. Line 38 assigns the addition of first i.e. the value of the first 8-bit and the processed value for second i.e. the upper 4-bit to the public function ADC (). These values represent the converted value for the entire 12-bit data from the analogue-to-digital converter. Line 39 terminates the operation and the final result in the function ADC () is sent to another sub programme that further processes it.

Appendix C gives the entire programme for the control and shows how the data read is processed before the final screen display.



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EMDI AKURE

dodo

ODOTRONICS

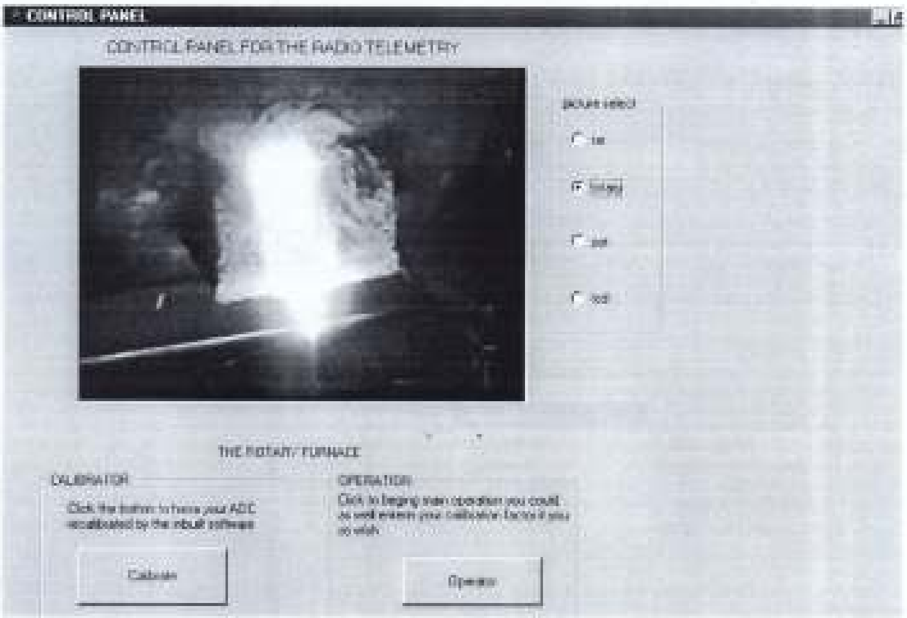
Version 1.0.0

Copyright : [illegible] 2001

Company : ODOTRONICS

Warning : This product is protected by the copy right law of the Federal Republic of Nigeria all right reserved to EMDI km 4 ondo road Akure Ondo State

Fig. 3.7: Product ID flash form



CONTROL PANEL FOR THE RADIO TELEMETRY

CALIBRATOR

Click the button to have your ADC recalibrated by the inbuilt software

OPERATION

Click to begin main operation you could as well esteem your calibration factor if you so wish

Fig.3.8: Main control panel

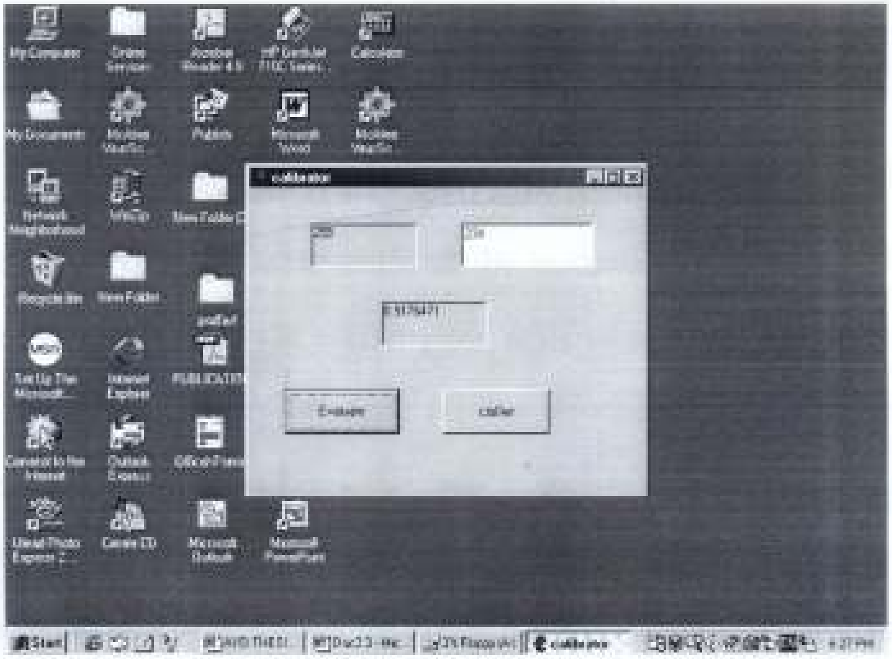
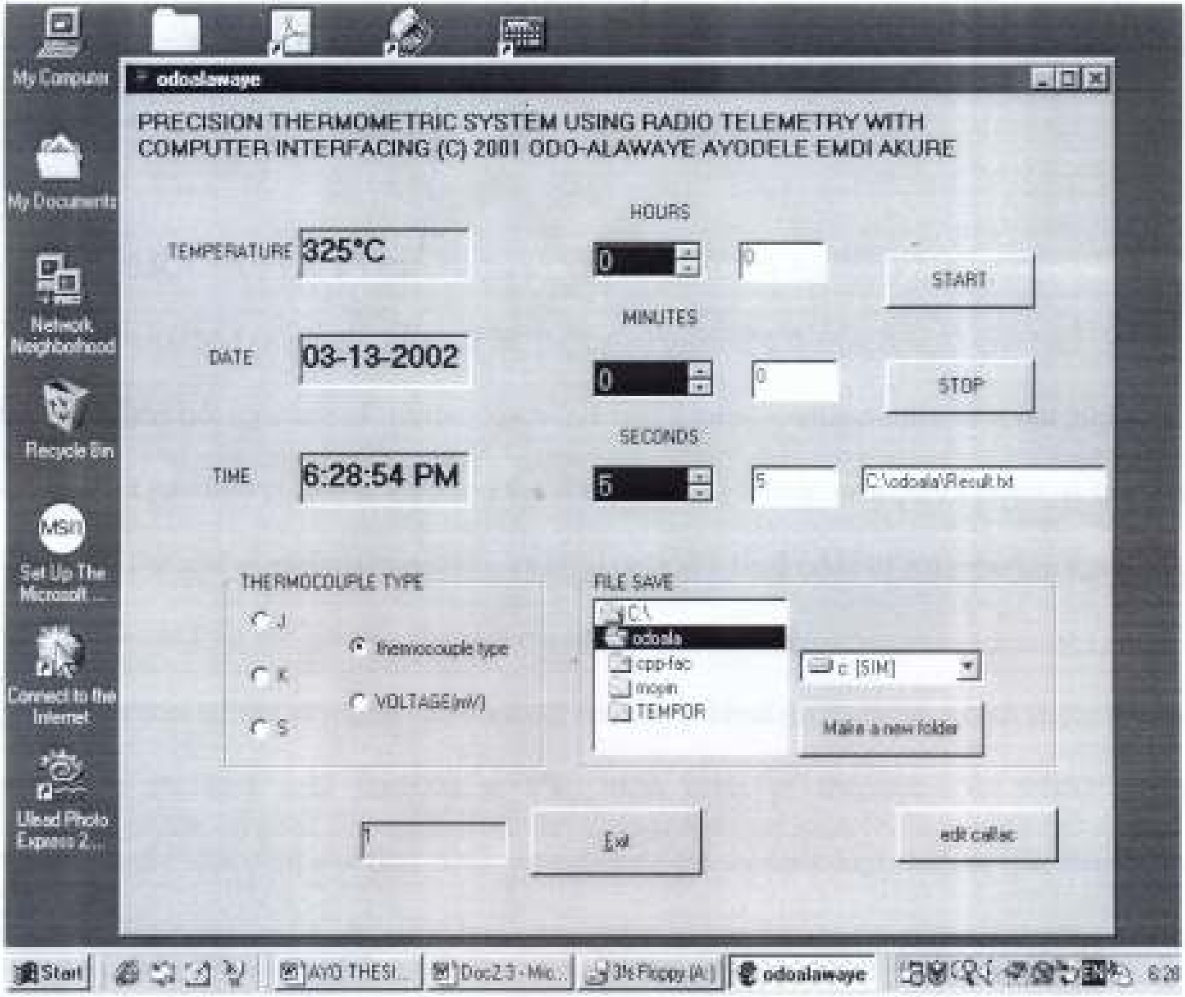


Fig.3.9: Recalibration form for ADC



odoalawaye

PRECISION THERMOMETRIC SYSTEM USING RADIO TELEMETRY WITH COMPUTER INTERFACING (C) 2001 ODO-ALAWAYE AYODELE EMDI AKURE

TEMPERATURE 325°C

DATE 03-13-2002

TIME 6:28:54 PM

HOURS 0 0

MINUTES 0 0

SECONDS 5 5

C:\odoala\Result.txt

THERMOCOUPLE TYPE

○ J

○ K

○ S

● thermocouple type

○ VOLTAGE(mV)

FILE SAVE

C:\

odoala

cpp-fac

mopin

TEMPOR

c: [SIM]

1

Fig.3.10: Data processing\logging control form

CHAPTER FOUR

RESULTS AND DISCUSSION

The circuitry for the achievement of the requirement of the project i.e. Precision thermometric system using radio telemetry was designed and first simulated on a computer using two electronics software packages; (1) The electronics work Bench and (2) Circuit maker. These are software packages that help to analyse an electronic circuit design and indicate the workability before implementing.

The actual implementation of the design was carried out in phases on different vero boards and each section of the entire design was tested separately before the final coupling and calibration. This chapter presents the experimental procedure and the results of the various tests carried out on each section of the design and concluding comments about all modifications on the initial design.

4.1 THERMOCOUPLE TYPE (Platinum Vs Platinum10% Radium)

The method generally adopted for the calibration of a thermocouple involves the dipping of the hot junction of the thermocouple into a known temperature of about 200°C, and its cold junction placed at 0°C, and the emf produced is read on a panel meter. A repeated reading of the emf at various temperatures is taken and a final table of temperature against emf is presented for the specific thermocouple. (www.omega.com/pdf/temperature/z/zsection.asp.).

Because of the stringent requirement for this calibration exercise which in most cases requires a standard cold junction at 0°C, most users of thermocouple relied on the manufacturers' standard and thus need not calibrate the thermocouple before use. Instead the output emf is compared with a standard table given in handbooks for thermocouples. For the purpose of this work the table presented in Appendix A, which is a standard for a type S thermocouple was used.

4.2 THERMOCOUPLE AMPLIFIER TEST RESULT

The thermocouple amplifier which forms a part of the analogue circuit presented in Fig 3.1 was set to a gain of 100 using the trimmer resistor *RV2*. For the test, a varying d.c. voltage of between 0 and 15.0mV was applied at the input of the thermocouple amplifier. This simulates the input voltage expected to cover the 'S' thermocouple range and the corresponding output voltage was measured with a digital voltmeter. The input and output voltage readings are shown in Table 4.1

The thermocouple amplifier was observed to produce a high response time and stable output whose drift with time is very small. The observerd linearity as shown in Fig 4.1 shows that the thermocouple amplifier meets the required standard desired for precise measurement.The slope of the graph shows the gain to be constant at 100_over the entire measurement range.

Table 4.1: Thermocouple amplifier characteristics with its gain set at 100

INPUT VOLTAGE (mV)	OUTPUT VOLTAGE (mV) at 27^0C
0.3	31
1.0	100
1.5	152
2.0	201
3.0	301
4.0	399
5.0	498
6.0	599
7.0	700
9.0	899
10.0	1000
12.0	1200
14.0	1398

4.3 VOLTAGE TO FREQUENCY CONVERTER TEST RESULT

The V/F converter, which also forms a major part of the circuit in Fig 3.1, was tested by applying the output from the thermocouple amplifier to the input of the converter at pin 7 of the LM331 through a 100k and 10nF capacitor cobination which help to remove any form of ripple in the thermocouple amplifier output voltage. Refering to Fig.3.2 a digital voltmeter was connected to point L to measure the input voltage to the converter and a digital frequency meter was connected to point M to measure the output frequency. Table 4.2 shows the result of the test. It was observed that the converter is very stable with little drift with variation of ambient tenperature, which was corrected for by replacing the capacitors C7 in the converter circuit, which was initially an electrolytic capacitor with a ceramic of same capacitance, since the capacitance of a ceramic capacitors is not seriously effected by variation of ambient temperature

Fig. 4.2 is a plot of the result of Table 4.2. It demonstrates good linearity of the V/F converters, and thus satisfies the required standard for the design. The slope from the graph shows the conversion ratio to meet the required 1 *kHz/V*.

Table 4.2: V/F frequency output trimmed at a conversion factor of 1Hz/mV

THERMOCOUPLE AMP OUTPUT VOLTAGE (v)	V/F OUTPUT FREQUENCY (kHz)
0.09	0.11
0.21	0.20
0.30	0.29
0.40	0.41
0.51	0.50
0.60	0.60
0.69	0.71
0.80	0.79
0.92	0.92
1.00	1.02
1.09	1.11
1.21	1.20
1.29	1.28
1.40	1.41
1.52	1.51

4.4 TRANSMITTER, RECEIVER AND FREQUENTCY-TO-VOLTAGE CONVERTER TEST RESULT

The next test was carried out by coupling the entire components of the circuit as shown in Fig 3.2. The output from the voltage-to-frequency converter i.e. pin 3 of the LM331 and the variable resistor *R15* used to trim the modulating voltage to the FM transmitter. An FM receiver set at about 220MHz on the VHF band was used to demodulate the transmitted signal. Clear reception of transmitted signal was obtained at about 20 meter radius from the transmitting point, which is adequate for this work as applied for the monitoring of a rotary furnace temperature. After reception, the demodulated signal was then fed into the frequency-to-voltage converter i.e. pin 6 of the LM331 used in this case as a F/V converter through two inverter that provides the 5Vp-p pulse necessary to drive the converter. The demodulated frequency was measured with a digital frequency counter connected to the point N while the corresponding output voltage from the Frequency-to-Voltage converter (after buffered by the unity gain amplifier *U2*) was measured with a digital voltmeter connected to point O. The results obtained are shown in Table 4.3

It was observed that as the input frequency into the transmitter increases there was a slight upward shift of about 20MHz in the transmitter's center frequency which was reduced to a bearable limit by reducing the modulation voltage through the R15 variable pot. The plot of the results of Table.4.3 shown in Fig 4.3 establishes the linearity of the network.

Table 4.3: output result for the receiver and F/V converter

MODULATION FREQUENCY (kHz)	DEMODULATED FREQUENCY	VOLTAGE OUTPUT F/V CONVERTER in (V)
0.05	0.06	0.05
0.10	0.11	0.11
0.19	0.20	0.20
0.30	0.29	0.30
0.41	0.40	0.40
0.51	0.50	0.51
0.78	0.79	0.78
1.01	1.00	1.00
1.21	1.21	1.22
1.39	1.40	1.39
1.52	1.51	1.52

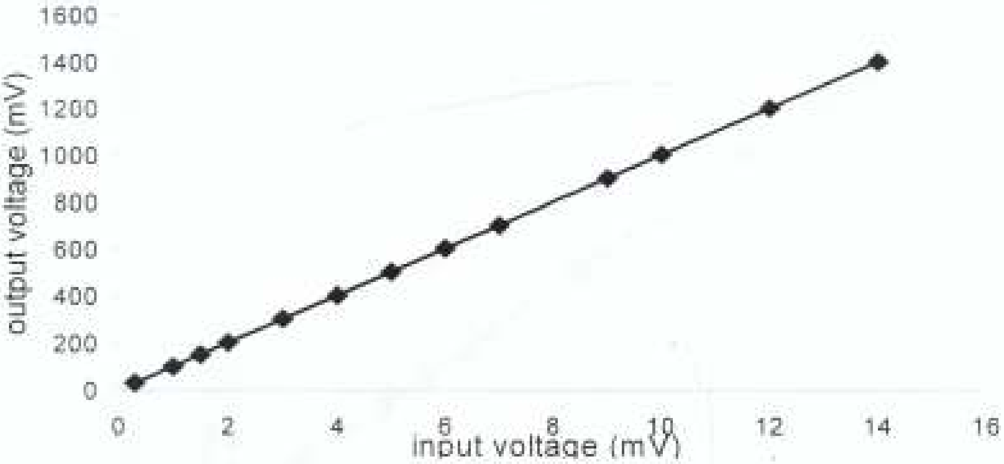


Fig.4.1: The thermocouple amplifiers output voltage versus input voltage

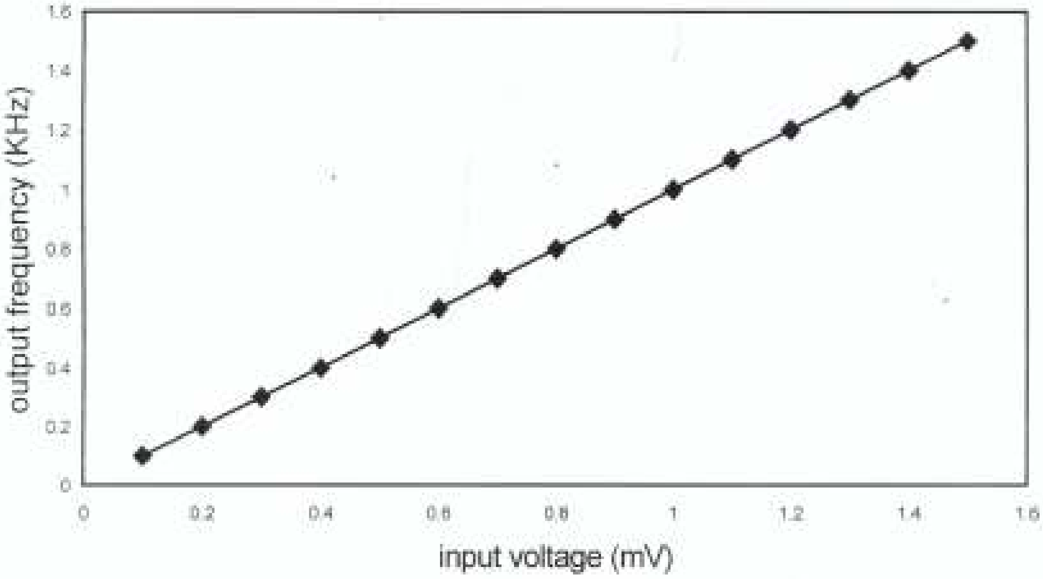


Fig.4.2: The V/F converter output frequency versus input voltage

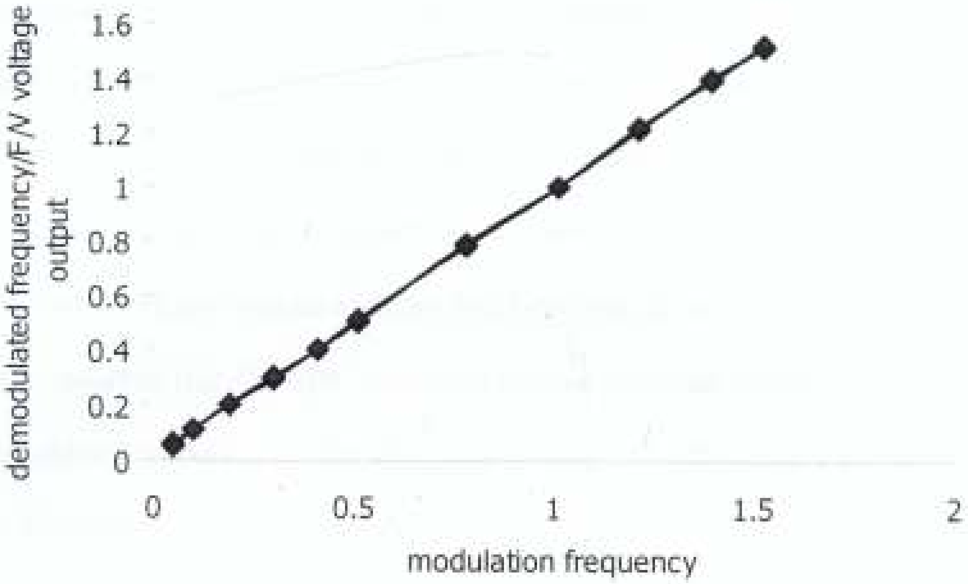


Fig 4.3: A plot of demodulated frequency/output voltage versus the modulating frequency

4.5 COMPUTER INTERFACE ADAPTER AND PROGRAMME TEST

This network which consists of the 12-bit analogue-to-digital converter was both hardware and software calibrated to ensure its integrity. For the hardware circuit calibration and test, a known voltage was applied to the circuit shown in Fig 3.5. The corresponding binary output decoded by means of 12 LEDs was then observed. The pot *RV1* was used to adjust the reference voltage until an accuracy of ±1-bit was achieved for all input voltage.

It was observed that the ADC generated internal heat that put the device temperature at 42°C after about 10 minutes of operation. The accuracy of convertion was not observed to be effected. The table 4.4 presents the results of the test.

The integrity of the software was tested by connecting the device through the printer's port and the control programme was run. Referring to Fig 3.7 through 3.10, first a known input voltage was placed at the input of the ADC, a subprogramme called calibrator was activated. The value of the input voltage was entered into a textbox and then the return button was pressed. The programme then compared the user's entered value with the value decoded from a read operation from the printers port and performs the operation (input voltage by user/ converted voltage from the port) to generate a correcting factor that acted as a multiplier to all other converted readings from the port. These compensated for errors that could arise due to effect of change in environmental condition after the initial hardware calibration and the non-linearity of the thermocouple. The output result was displayed on the graphical screen and results retrieved of the data logged showed that the software worked as expected with an accuracy of ±1°C. The programme for the callibration written in Visual Basic is presented in Appendix C.

Table 4.5: The analogue to digital converter output

INPUT VOLTAGE (mV)	LED's DISPLAY OUTPUT											
	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
10	0	0	0	0	0	0	0	0	1	0	1	1
50	0	0	0	0	0	0	1	1	0	0	1	0
100	0	0	0	0	0	1	1	0	0	1	0	0
200	0	0	0	0	1	1	0	0	1	0	0	0
300	0	0	0	1	0	0	1	0	1	1	0	0
400	0	0	0	1	1	0	0	1	0	0	0	1
500	0	0	0	1	1	1	1	1	0	1	0	0
600	0	0	1	0	0	1	0	1	1	0	0	0
800	0	0	1	1	0	0	1	0	0	0	0	0
1000	0	0	1	1	1	1	1	0	1	0	0	1
1200	0	1	0	0	1	0	1	1	0	0	0	0
1400	0	1	0	1	0	1	1	1	1	0	0	0
1500	0	1	0	1	1	1	0	1	1	1	0	1

1	**Indicates that the LED is ON**
0	**Indicates that the LED is OFF**

4.6 STANDARD AND EVALUATION TEST

In order to fully ascertain the integrity of the system the entire circuit was used to monitor the temperature in an electric furnace (Muffle) manufactured by Gallenhamp Corporation UK. It has its own in built temperature measuring device. The temperature as displayed on the visual display unit of the computer was compared with that of the furnace temperature display. The result is as presented in table 4.6, for temperature in the range 50°C to 1200°C which is the entire temperature range for the electric furnace. It was observed thet the system tracks the displayed furnace temperature accurately and the response time (i.e. time laps in the response of the tested to the referenced temperature measuring device) was less than 2seconds which is just adequate.

Table 4.6: Temperature output as read from the furnace and the constructed thermometry system

ELECTRIC FURNACE TEMPERATURE (°C)	TEMPERATURE DISPLAYED BY THE THERMOMETRY SYSTEM (°C)
50	50
100	101
200	201
300	302
400	401
500	502
600	600
700	699
800	799
900	901
1000	1001
1100	1102

4.7 OPERATION AND PERFORMANCE OF THE SYSTEM

The effectiveness and utility performance of the system has been tested for monitoring the temperature of a rotary furnace (EMR100) of the Engineering Materials Development Institute, Akure, used for melting cast iron over the temperature range 50 to 1400°C. The test carried out over a long period has the first module i.e. the transmitting circuitry attached directly to the rotating furnace. The system was found to be stable when the VHF receiver was properly tuned for best reception, little drift due to transmission losses, which demanded a constant re-tuning of the receiver was however observed. This drift could be associated with the effect of air current around the rotary furnace body (Vidyallal et al., 1993), and which can affect the inductance of the oscillating tank in the transmitter section. Other forms of anticipated errors are the input offset voltage of *U1*, the cold-junction compensation mismatch and change in the value of the resistors with temperature.

4.8 CONCLUSION AND RECOMMENDATION

It has been demonstrated that the measurement of physical parameters such as temperature in an inaccessible or hazardous environment is indeed possible with radio telemetry. The advantage of this scheme over other well-known means of high temperature measurement systems like optical pyrometer is evident in its stability. That is its consistency in the measured output and the fact that results of such output can be accurately recorded at a distance far away from the system whose temperature is being monitored. Although the maximum distance apart for the accurate application of this device has not been established, it does satisfy our design limit of 20 meters, it is indeed possible to increase the range by improving on the transmitter power.

The adaptability of a personal computer for the purpose of processing and data logging large amounts of data at great speed and also carrying out difficult computational process on such data with results displayed almost immediately on the VDU therefore presents a cheap means of achieving complex control with ease. This inherent great potential may result into further research for design of dedicated integrated measurement/control system for adaptability to various transducers (active or passive) employed in measurement and instrumentation.

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APPENDIX A

STANDARD CALLIBRATION TABLE FOR THERMOCOUPLE
HANDBOOK OF CHEMISTRY AND PHYSICS 62nd EDITION 1981-1982

STANDARD CALIBRATION TABLES FOR THERMOCOUPLES

The following tables which represent the Temperature-E.M.F. functions of various thermocouples should be used with appropriate corr curves if precise results are desired. These curves must be determined for each individual couple by plotting ΔE, the difference betwe observed and the standard E.M.F., against the standard E.M.F. at three or more fixed temperature points. The value ΔE as shown by correction curve is then subtracted algebraically from the observed E.M.F. to give the true E.M.F. reading.

In the following tables the fixed or "cold junction" is at 0°C.; when the cold junction is not maintained at 0°C. the readings of the E must be corrected as follows: $Et = E_{t_1 \ldots t_1} + Etc$ where $E_{t_1 \ldots t_1}$ is the observed reading, *Etc* is the E.M.F. for the temperature correspond the cold junction temperature as read from the standard table and *Et* is the E.M.F. produced by the jot junction corrected to the value would be obtained with the cold junction at 0°C. The temperature corresponding to *Et* is then obtained by reference to the standard table.

Since the E.M.F.-temperature function is not linear the cold junction should be maintained at a temperature very close to that at wh thermocouple was calibrated. Otherwise considerable error will result despite the above correction.

PLATINUM VERSUS PLATINUM-10-PERCENT RHODIUM THERMOCOUPLES

(Electromotive Force in Absolute Millivolts. Temperatures in Degrees C (Int. 1948). Reference Junctions at 0°C.)

°C	0	10	20	30	40	50	60	70	80	90
					Millivolts					
0	0	0.06	0.11	0.17	0.24	0.30	0.36	0.43	0.50	0.57
100	0.64	0.72	0.79	0.87	0.95	1.03	1.11	1.19	1.27	1.35
200	1.44	1.52	1.61	1.69	1.78	1.87	1.96	2.05	2.14	2.23
300	2.32	2.41	2.50	2.59	2.69	2.78	2.87	2.97	3.06	3.16
400	3.25	3.35	3.44	3.54	3.64	3.73	3.83	3.93	4.02	4.12
500	4.22	4.32	4.42	4.52	4.62	4.72	4.82	4.92	5.02	5.12
600	5.22	5.33	5.43	5.53	5.64	5.74	5.84	5.95	6.05	6.16
700	6.26	6.37	6.47	6.58	6.68	6.79	6.90	7.01	7.11	7.22
800	7.33	7.44	7.55	7.66	7.77	7.88	7.99	8.10	8.21	8.32
900	8.43	8.55	8.66	8.77	8.88	9.00	9.11	9.23	9.34	9.46
1000	9.57	9.6	9.80	9.92	10.04	10.15	10.27	10.39	10.51	10.62
1100	10.74	10.86	10.98	11.10	11.22	11.34	11.46	11.58	11.70	11.82
1200	11.94	12.06	12.18	12.30	12.42	12.54	12.66	12.78	12.90	13.02
1300	13.14	13.26	13.38	13.50	13.62	13.74	13.86	13.98	14.10	14.22
1400	14.34	14.46	14.58	14.70	14.82	14.94	15.05	15.17	15.29	15.41
1500	15.53	15.65	15.77	15.89	16.01	16.12	16.24	16.36	16.48	16.60
1600	16.72	16.83	16.95	17.07	17.19	17.31	17.42	17.54	17.66	17.77
1700	17.89	18.01	18.12	18.24	18.36	18.47	18.59	—	—	—

(Electromotive Force in Absolute Millivolts. Temperatures in Degrees F.* Reference Junctions at 32°F.)

°F	0	10	20	30	40	50	60	70	80	90
					Millivolts					
0	—	—	—	—	0.02	0.06	0.09	0.12	0.15	0.19
100	0.22	0.26	0.29	0.33	0.36	0.40	0.44	0.48	0.52	0.56
200	0.60	0.64	0.68	0.72	0.76	0.80	0.84	0.89	0.93	0.97
300	1.02	1.06	1.11	1.15	1.20	1.24	1.29	1.33	1.38	1.43
400	1.47	1.52	1.57	1.62	1.66	1.71	1.76	1.81	1.86	1.91
500	1.96	2.01	2.06	2.11	2.16	2.21	2.26	2.31	2.36	2.41
600	2.46	2.51	2.56	2.61	2.66	2.72	2.77	2.82	2.87	2.92
700	2.98	3.03	3.08	3.14	3.19	3.24	3.29	3.35	3.40	3.45
800	3.51	3.56	3.61	3.67	3.72	3.78	3.83	3.88	3.94	3.99
900	4.05	4.10	4.16	4.21	4.26	4.32	4.37	4.43	4.49	4.54
1000	4.60	4.65	4.71	4.76	4.82	4.87	4.93	4.99	5.04	5.10
1100	5.16	5.21	5.27	5.33	5.38	5.44	5.50	5.56	5.61	5.67
1200	5.73	5.78	5.84	5.90	5.96	6.02	6.07	6.13	6.19	6.25
1300	6.31	6.37	6.42	6.48	6.54	6.60	6.66	6.72	6.78	6.84
1400	6.90	6.96	7.02	7.08	7.14	7.20	7.26	7.32	7.38	7.44
1500	7.50	7.56	7.62	7.68	7.74	7.80	7.86	7.93	7.99	8.05
1600	8.11	8.17	8.23	8.30	8.36	8.42	8.48	8.55	8.61	8.67
1700	8.73	8.80	8.86	8.92	8.98	9.05	9.11	9.17	9.24	9.30
1800	9.37	9.43	9.49	9.56	9.62	9.69	9.75	9.82	9.88	9.94
1900	10.01	10.07	10.14	1.20	10.27	10.33	10.40	10.47	10.53	10.60
2000	10.66	10.73	10.79	10.86	10.93	10.99	11.06	11.12	11.19	11.26

PLATINUM VERSUS PLATINUM-1 PERCENT RHODIUM THERMOCOUPLES

(Electromotive Force in Absolute Millivolts. Temperatures in Degrees C (Int. 1948) Reference Junctions at 0°C.)

°C	0	10	20	30	40	50	60	70	80
					Millivolts				
0	0.00	0.06	0.11	0.17	0.23	0.30	0.36	0.43	0.50
100	0.65	0.72	0.80	0.88	0.96	1.04	1.12	1.21	1.29
200	1.47	1.55	1.64	1.73	1.83	1.92	2.01	2.11	2.20
300	2.40	2.49	2.59	2.69	2.79	2.89	2.99	3.09	3.19
400	3.40	3.50	3.61	3.71	3.82	3.92	4.03	4.13	4.24
500	4.46	4.56	4.67	4.78	4.89	5.00	5.12	5.23	5.34
600	5.56	5.68	5.79	5.91	6.02	6.14	6.25	6.37	6.49
700	6.72	6.84	6.96	7.08	7.20	7.32	7.44	7.56	7.68
800	7.92	8.05	8.17	8.29	8.42	8.54	8.67	8.80	8.92
900	9.18	9.30	9.43	9.56	9.69	9.82	9.95	10.08	10.21
1000	10.47	10.60	10.74	10.87	11.00	11.14	11.27	11.41	11.54
1100	11.82	11.94	12.09	12.23	12.37	12.50	12.64	12.78	12.92
1200	13.19	13.33	13.47	13.61	13.75	13.89	14.03	14.17	14.30
1300	14.58	14.72	14.86	15.00	15.14	15.28	15.42	15.55	15.69
1400	15.97	16.11	16.25	16.39	16.52	16.66	16.80	16.94	17.08
1500	17.36	17.49	17.63	17.77	17.91	18.04	18.18	18.32	18.45
1600	18.73	18.86	19.00	19.14	19.27	19.41	19.55	19.68	19.82
1700	20.09	—	—	—	—	—	—	—	—

(Electromotive Force in Absolute Millivolts. Temperatures in Degrees F* Reference Junctions at 32°F.)

°F	0	10	20	30	40	50	60	70	80
					Millivolts				
0	—	—	—	—	0.02	0.06	0.09	0.12	0.15
100	0.22	0.26	0.29	0.33	0.36	0.40	0.44	0.48	0.52
200	0.60	0.64	0.68	0.72	0.76	0.81	0.85	0.89	0.94
300	1.03	1.08	1.12	1.17	1.21	1.26	1.31	1.36	1.41
400	1.50	1.55	1.60	1.65	1.70	1.75	1.81	1.86	1.91
500	2.01	2.07	2.12	2.17	2.22	2.28	2.33	2.38	2.44
600	2.55	2.60	2.66	2.71	2.77	2.82	2.88	2.94	2.99
700	3.10	3.16	3.22	3.27	3.33	3.39	3.45	3.50	3.56
800	3.68	3.74	3.79	3.85	3.91	3.97	4.03	4.09	4.14
900	4.26	4.32	4.38	4.44	4.50	4.56	4.62	4.69	4.75
1000	4.87	4.93	4.99	5.05	5.12	5.18	5.24	5.30	5.36
1100	5.49	5.55	5.61	5.68	5.74	5.81	5.87	5.93	6.00
1200	6.13	6.19	6.25	6.32	6.38	6.45	6.51	6.58	6.64
1300	6.77	6.84	6.90	6.97	7.04	7.10	7.17	7.24	7.30
1400	7.44	7.50	7.57	7.64	7.71	7.77	7.84	7.91	7.98
1500	8.12	8.18	8.25	8.32	8.39	8.46	8.53	8.60	8.67
1600	8.81	8.88	8.95	9.02	9.09	9.16	9.23	9.30	9.37
1700	9.52	9.59	9.66	9.73	9.80	9.87	9.95	10.02	10.09
1800	10.24	10.31	10.38	10.46	10.53	10.60	10.68	10.75	10.82
1900	10.97	11.05	11.12	11.20	11.27	11.35	11.42	11.50	11.58
2000	11.73	11.80	11.88	11.95	12.03	12.11	12.18	12.26	12.34

APPENDIX B

LM331 V/F AND F/V CONVERTER APPLICATION NOTE
NATIONAL SEMICONDUCTOR INC

V/F Converter ICs Handle Frequency-to-Voltage Needs

National Semiconductor
Appendix C
Robert A. Pease
August 1980

Simplify your F/V converter designs with versatile V/F ICs. Starting with a basic converter circuit, you can modify it to meet almost any application requirement. You can spare yourself some hard labor when designing frequency-to-voltage (F/V) converters by using a voltage-to-frequency IC in your designs. These ICs form the basis of a series of accurate, yet economical, F/V converters suiting a variety of applications.

Figure 1 shows an LM331 IC (or LM131 for the military temperature range) in a basic F/V converter configuration (sometimes termed a stand-alone converter because it requires no op amps or other active devices other than the IC). (Comparable V/F ICs, such as RM4151, can take advantage of this and other circuits described in this article, although they might not always be pin-for-pin compatible).

This circuit accepts a pulse-train or square wave input amplitude of 3V or greater. The 470 pF coupling capacitor suits negative-going input pulses between 80 μs and 1.5 μs, as well as accommodating square waves or positive-going pulses (as long as the interval between pulses is at least 10 μs).

IC Handles the Hard Part

The LM331 detects an input-signal change by sensing when pin 6 goes negative relative to the threshold voltage at pin 7, which is nominally biased 2V lower than the supply voltage. When a signal change occurs, the LM331's input comparator sets an internal latch and initiates a timing cycle. During this cycle, a current equal to V_{REF}/R_S flows out of pin 1 for a time $t = 1.1\, R_tC$. The 1 μF capacitor filters the pulsating current from pin 1, and the current's average value flows through load resistor R_L. As a result, for a 10 kHz input, the circuit outputs 10 V_{DC} across R_L with good (0.06% typical) nonlinearity.

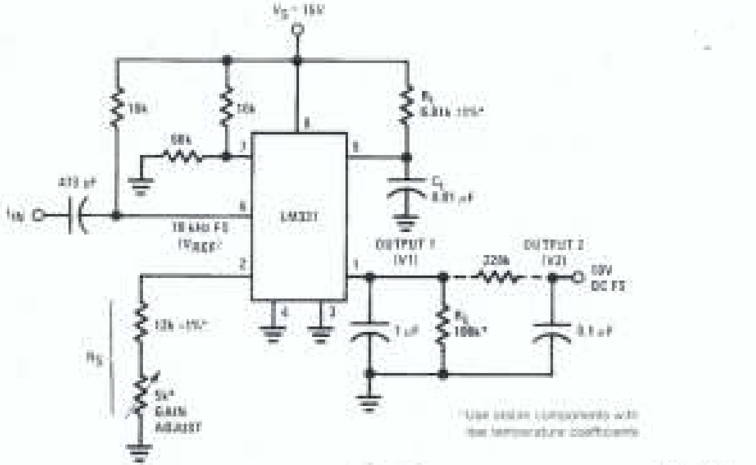
Two problems remain, however: the output at V1 includes about 13 mVp-p ripple, and it also lags 0.1 second behind an input frequency step change, settling to 0.1% of full-scale in about 0.6 second. This ripple and slow response represent an inherent tradeoff that applies to almost every F/V converter.

The Art of Compromise

Increasing the filter capacitor's value reduces ripple but also increases response time. Conversely, lowering the filter capacitor's value improves response time at the expense of larger ripple. In some cases, adding an active filter results in faster response and less ripple for high input frequencies.

Although the circuit specifies a 15V power supply, you can use any regulated supply between 4 V_{DC} and 40 V_{DC}. The output voltage can extend to within 3 V_{DC} of the supply voltage, so choose R_L to maintain that output range.

Adding a 220 kΩ/0.1 μF postfilter to the circuit slows the response slightly, but it also reduces ripple to less than 1 mVp-p for frequencies from 200 Hz to 10 kHz. The reduction in ripple achieved by adding this passive filter, while not as good as that obtainable using an active filter, could suffice in some applications.



*Use stable components with low temperature coefficients

TL/H/8141-1

FIGURE 1. A Simple Stand-Alone F/V Converter Forms the Basis for Many Other Converter-Circuit Configurations

Improving the Basic Circuit

Further modifications and additions to the basic F/V converter shown in *Figure 1* can adapt it to specific performance requirements. *Figure 2* shows one such modification, which improves the converter's nonlinearity to 0.006% typical.

Reconsideration of the basic stand-alone converter shows why its nonlinearity falls short of this improved version's. At low input frequencies, the current source feeding pin 1 in the LM331 is turned off most of the time. As the input frequency increases, however, the current source stays on more of the time, and its own impedance attenuates the output signal for an increasing fraction of each cycle time. This disproportionate attenuation at higher frequencies causes a parabolic change in full-scale gain rather than the desired linear one.

In the improved circuit, on the other hand, the PNP transistor acts as a cascade, so the output impedance at pin 1 sees a constant voltage that won't modulate the gain. Also, with an alpha ranging between 0.998 and 0.990, the transistor exhibits a temperature coefficient of between 10 ppm/°C and 40 ppm/°C—a fairly minor effect. Thus, this circuit's nonlinearity does not exceed 0.01% maximum for the 10V output range shown and is normally not worse than 0.01% for any supply voltage between 4V and 40V.

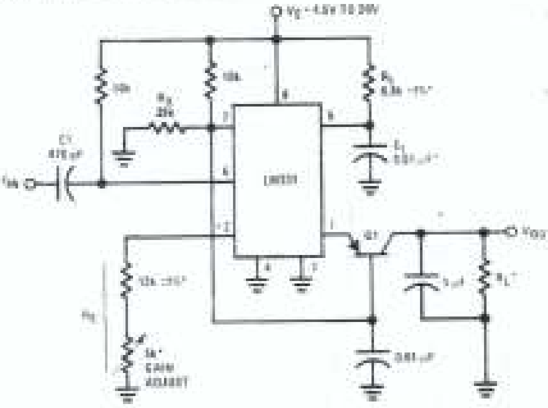
Add an Output Buffer

The circuit in *Figure 3* adds an output buffer (unity-gain follower) to the basic single-supply F/V converter. Either an LM324 or LM358 op amp functions well in a single-supply circuit because these devices' common-mode ranges extend down to ground. But if a negative supply is available, you can use any op amp; types such as the LF351B or LM308A, which have low input currents, provide the best accuracy.

The output buffer in *Figure 3* also acts as an active filter, furnishing a 2-pole response from a single op amp. This filter provides the general response

$$V_{OUT}/I_{OUT} = R_L/(1 + K1p + K2p^2).$$

(p is the differential operator d/dt.) As shown, R_L controls the filter's DC gain. The high frequency response rolls off at 12 dB/octave. Near the circuit's natural resonant frequency, you can choose the damping to give a little overshoot—or none, as desired.

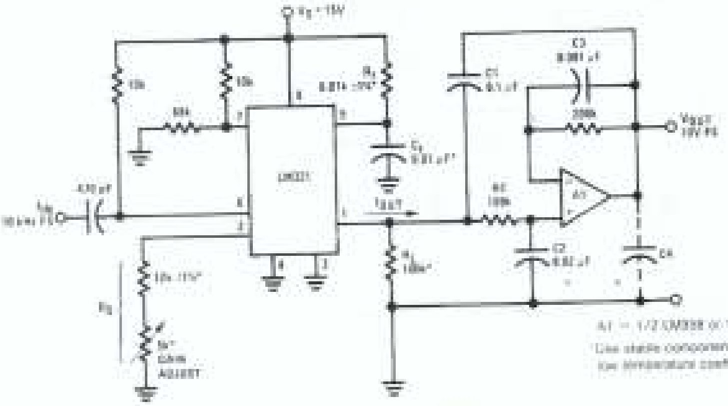


Q1 = 2N4250, 2N3906 or similar high-beta PNP transistor

Select R1 = (VS − 2V)/(2V) × 10 kΩ

*Use stable components with low temperature coefficients

FIGURE 2. Adding a Cascade Transistor to the LM331's Output Improves Nonlinearity to 0.006%



A1 = 1/2 LM358 or 1/4 LM324

*Use stable components with low temperature coefficients

FIGURE 3. The Op Amp on This F/V Converter's Output Acts as a Buffer as Well as a 2-Pole Filter

Dealing with F/V Converter Ripple

Voltage ripple on the output of F/V converters can present a problem, and the chart shown in *Figure A* indicates exactly how big a problem it is. A simple, slow, RC filter exhibits low ripple at all frequencies. Two-pole filters offer the lowest ripple at high frequencies and provide a 30-times-faster step response than RC devices.

To reduce a circuit's ripple at moderate frequencies, however, you can cascade a second active-filter stage on the F/V converter's output. That circuit's response also appears in *Figure A* and shows a significant improvement in low-ripple bandwidth over the single-active-filter configuration, with only a 30% degradation of step response.

Figures B and *C* show filter circuits suitable for cascading. The inverting filter in *Figure B* requires closely matched resistors with a low TC over their temperature range for best accuracy. For lowest DC error, choose $R5 = R2 + (R_{IN}||R_F)$. This circuit's response is

$$-V_{OUT}/V_{IN} = n/(1 + (R_F + R2 + nR2)C4p + R_FR2C3C4p^2),$$

where n = DC gain. If $R_{IN} = R_F$ and n = 1,

$$-V_{OUT}/V_{IN} = 1/(1 + (R_F + 2R2)C4p + R_FR2C3C4p^2).$$

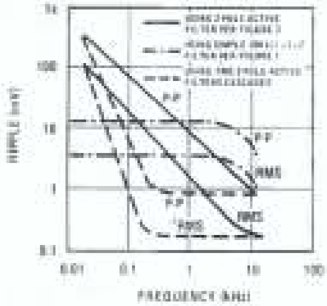


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FIGURE A. Output-Ripple Performance of Several Different F/V Converter Configurations Illustrates the Effect of Voltage Ripple

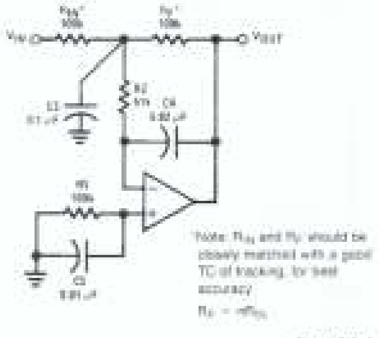

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FIGURE B. You Can Cascade This 2-Pole Inverting Filter onto an F/V Converter's Output

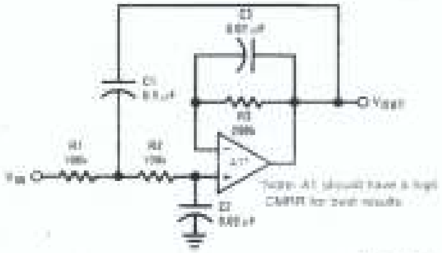

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FIGURE C. This 2-Pole Noninverting Filter Suits Cascade Requirements on F/V Converter Outputs

The circuit shown in *Figure C* does not require precision passive components, but for best accuracy, choosing an A1 with a high CMRR is critical. An LM308A op amp's 96 dB minimum CMRR suits this circuit well, but an LM358B's 85 dB typical figure also proves adequate for many applications. Circuit response is

$$V_{OUT}/V_{IN} = 1/(1 + (R1 + R2)C2p + R1R2C1C2p^2).$$

For best results, choose R3 = R1 + R2.

Components Determine Response

The specific response of the circuit in *Figure 3* is

$$V_{OUT}/I_{OUT} = R_L/(1 + (R_L + R2)C2p + R_LR2C1C2C2p^2).$$

Making C2 relatively large eliminates overshoot and sine peaking. Alternatively, making C2 a suitable fraction of C1 (as is done in *Figure 3*) produces both a sine response with 0 dB to 1 dB of peaking and a quick real-time response having only 10% to 30% overshoot for a step response. By maintaining *Figure 3*'s ratio of C1:C2 and R2:R_L, you can adapt its 2-pole filter to a wide frequency range without tedious computations.

This filter settles to within 1% of a 5V step's final value in about 20 ms. By contrast, the circuit with the simple RC filter shown in *Figure 1* takes about 900 ms to achieve the same response, yet offers no less ripple than *Figure 3*'s op amp approach.

As for the other component in the 2-pole filter, any capacitance between 100 pF and 0.05 µF suits C3 because it serves only as a bypass for the 200 kΩ resistor. C4 helps reduce output ripple in single positive power-supply systems when V_{OUT} approaches so close to ground that the op amp's output impedance suffers. In this circuit, using a tantalum capacitor of between 0.1 µF and 2.2 µF for C4 usually helps keep the filter's output much quieter without degrading the op amp's stability.

Avoid Low-Leakage Limitations

Note that in most ordinary applications, this 2-pole filter performs as well with 0.1 µF and 0.02 µF capacitors as the passive filter in *Figure 1* does with 1 µF. Thus, if you require a 100 Hz F/V converter, the circuit in *Figure 2* furnishes good filtering with C1 = 10 µF and C2 = 2 µF, and eliminates the 100 µF low-leakage capacitor needed in a passive filter.

Note also that because C1 always has zero DC voltage across it, you can use a tantalum or aluminum electrolytic capacitor for C1 with no leakage-related problems; C2, however, must be a low-leakage type. At room temperature, typical 1 µF tantalum components allow only a few nanoamperes of leakage, but leakage this low usually cannot be guaranteed.

Compensating for Temperature Coefficients

F/V converters often encounter temperature-related problems usually resulting from the temperature coefficients of passive components. Following some simple design and manufacturing guidelines can help immunize your circuits against loss of accuracy when the temperature changes.

Capacitors fabricated from Teflon or polystyrene usually exhibit a TC of −110 ±30 ppm/°C. When you use such a component for the timing capacitor in an F/V converter (such as C_t in the *figure*) the circuit's output voltage—or the gain in terms of volts per kilohertz—also exhibits a −110 ppm/°C TC.

But the resistor-diode network (R_X, D1, D2) connected from pin 2 to ground in the *figure* can cancel the effect of the timing capacitor's large TC. When R_X = 240 kΩ, the current flowing through pin 1 will then have an overall TC of 110 ppm/°C, effectively canceling a polystyrene timing capacitor's TC to a first approximation. Thus, you needn't find a zero-TC capacitor for C_t so long as its temperature coefficient is stable and well established. As an additional advantage, the resistor-diode network nearly compensates to zero the TC of the rest of the circuit.

Bake it for a While

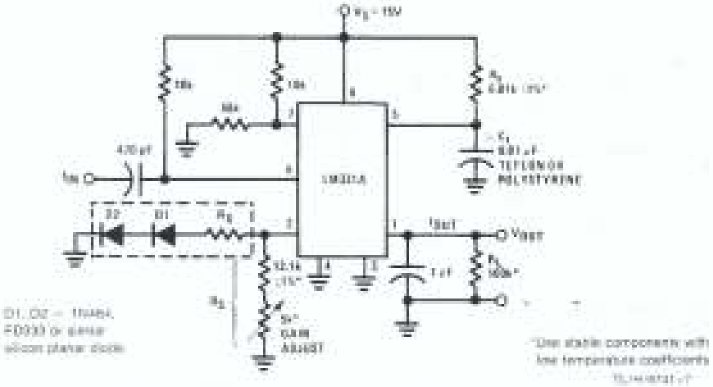
After the circuit has been built and checked out at room temperature, a brief oven test will indicate the sign and the size of the TC for the complete F/V converter. Then you can add resistance in series with R_X, or add conductance in parallel with it, to greatly diminish the TC previously observed and yield a complete circuit with a lower TC than you could obtain simply by buying low TC parts.

For example, if the circuit increases its full-scale output by 0.1% per 30°C (33 ppm/°C) during the oven test, adding 120 kΩ in series with R_X = 240 kΩ cancels the temperature-caused deviation. Or, if the full-scale output decreases by −0.04% per 20°C (−20 ppm/°C), just add 1.2 MΩ in parallel with R_X.

Note that to allow trimming in both directions, you must start with a finite *fixed* TC (such as the −110 ppm/°C of C_t), which then nominally cancels out by the addition of a finite *adjustable* TC. Only by using this procedure can you compensate for whatever polarity of TC is found by the oven test.

You can utilize this technique to obtain TCs as low as 20 ppm/°C, or perhaps even 10 ppm/°C, if you take a few passes to zero-in on the best value for R_X. For optimum results, consider the following guidelines:

- Use a good capacitor for C_t; the cheapest polystyrene capacitors can shift value by 0.05% or more per temperature cycle. In that case, you would not be able to distinguish the actual temperature sensitivity from the hysteresis, and you would also never achieve a stable circuit.
- After soldering, bake or temperature-cycle the circuit (at a temperature not exceeding 75°C in the case of polystyrene) for a few hours to stabilize all components and to relieve the strains of soldering.
- Do not rush the trimming. Recheck the room temperature value before *and* after you take the high temperature data to ensure a reasonably low hysteresis per cycle.
- Do not expect a perfect TC at −25°C if you trim for ±5 ppm/°C at temperatures from −25°C to 60°C. None of the components in the *figure's* circuit offer linearity much better than 5 ppm/°C or 10 ppm/°C cold, if trimmed for a zero TC at warm temperatures. Even so, using these techniques you can obtain a data converter with better than 0.02% accuracy and 0.003% linearity, for a ±20°C range around room temperature.
- Start out the trimming with R_X installed and its value near the design-center value (e.g., 240 kΩ or 270 kΩ), so you



Two Diodes and a Resistor Help Decrease an F/V Converter's Temperature Coefficient

will be reasonably close to zero TC; you will usually find the process slower if you start without any resistor, because the trimming converges more slowly.

- If you change R_X from 240 kΩ to 220 kΩ, do not pull out the 240 kΩ part and put in a new 220 kΩ resistor—you will get much more consistent results by adding a 2.4 MΩ resistor in parallel. The same admonition holds true for adding resistance in series with R_X.
- Use reasonably stable components. If you use an LM331A (±50 ppm/°C maximum) and RN55D film resistors (each ±100 ppm/°C) for R_L, R_t and R_S, you probably won't be able to trim out the resulting ±350 ppm/°C worst-case TC. Resistors with a TC specification of 25 ppm/°C usually work well. Finally, use the same resistor value (e.g., 12.1 kΩ ±1%) for both R_S and R_L when these resistors come from the same manufacturer's batch; their TC tracking will usually rate at better than 20 ppm/°C.

Whenever an op amp is used as a buffer (as in *Figure 3*), its offset voltage and current (±7.5 mV maximum and ±100 nA, respectively, for most inexpensive devices) can cause a ±17.5 mV worst-case output offset. If both plus and minus supplies are available, however, you can easily provide a symmetrical offset adjustment. With only one supply, you can add a small positive current to each op amp input and also trim one of the inputs.

Need a Negative Output?

If your F/V converter application requires a negative output voltage, the circuit shown in *Figure 4* provides a solution with excellent linearity (±0.003% typical, ±0.01% maximum). And because pin 1 of the LM331 always remains at 0 V_{DC}, this circuit needs no cascade transistor. (Note, however, that while the circuit's nonlinearity error is negligible, its ripple is not.)

The circuit in *Figure 4* offers a significant advantage over some other designs because the offset adjust voltage derives from the stable 1.9 V_{DC} reference voltage at pin 2 of the LM331; thus any supply voltage shifts cause no output shifts. The offset pot can have any value between 200 kΩ and 2 MΩ.

An optional bypass capacitor (C2) connected from the op amp's positive input to ground prevents output noise arising from stray noise pickup at that point; the capacitance value is not critical.

A Familiar Response

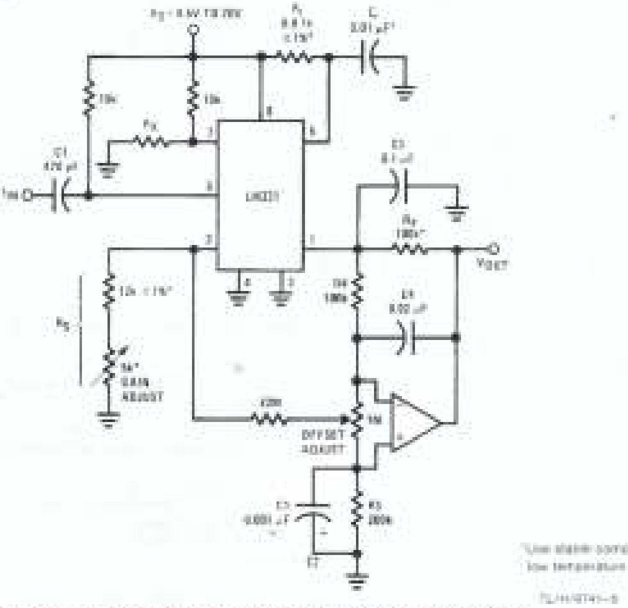
The circuit in *Figure 4* exhibits the same 2-pole response—with heavy output ripple attenuation—as the noninverting filter in *Figure 3*. Specifically,

$$V_{OUT}/f_{OUT} = R_F/(1 + (R_4 + R_F)C_4p + R_4R_FC_3C_4p^2).$$

Here also, R5 = R4 = R_F = 200 kΩ provides the best bias current compensation.

The LM331 can handle frequencies up to 100 kHz by utilizing smaller-value capacitors as shown in *Figure 5*. This circuit increases the current at pin 2 to facilitate high-speed switching, but, despite these speed-ups, the LM331's 500 ppm/°C TC at 100 kHz causes problems because of switching speed shifts resulting from temperature changes.

To compensate for the device's positive TC, the LM334 temperature sensor feeds pin 2 a current that decreases linearly with temperature and provides a low overall temperature coefficient. An R_Y value of 30 kΩ provides first-order compensation, but you can trim it higher or lower if you need more precise TC correction.



*Use stable components with low temperature coefficients.

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FIGURE 4. In This F/V Circuit, the Output-Buffer Op Amp Derives Its Offset Voltage from the Precision Voltage Source at Pin 2 of the LM331

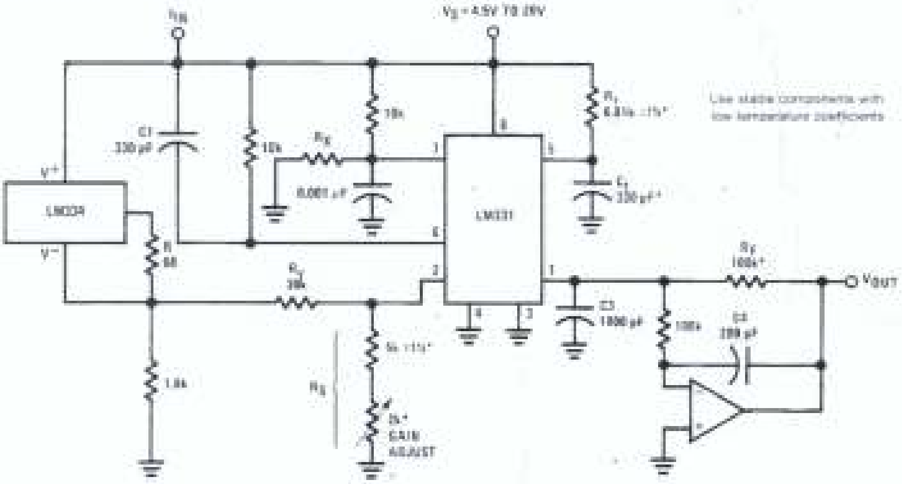
Detect Frequencies Accurately

Using an F/V converter combined with a comparator as a frequency detector is an obvious application for these devices. But when the F/V converter is utilized in this way, its output ripple hampers accurate frequency detection, and the slow filter frequency response causes delays.

If a quick response is not important, though, you can effectively utilize an LM331-based F/V converter to feed one or more comparators, as shown in *Figure 6*. For an input frequency drop from 1.1 kHz to 0.5 kHz, the converter's output responds within about 20 ms. When the input falls from 8 kHz to 0.9 kHz, however, the output responds only after a 600 ms lag; so utilize this circuit only in applications that can tolerate F/V circuits' inherent delays and ripples.

Author's Biography

Bob Pease is a staff scientist in the Advanced Linear Integrated Circuit Group at National Semiconductor Corp., Santa Clara, CA. Holder of four patents, he earned a BSEE from MIT. Bob lists tracking abandoned railroad roadbeds and designing V/F converters as hobbies.



*Use stable components with low temperature coefficients

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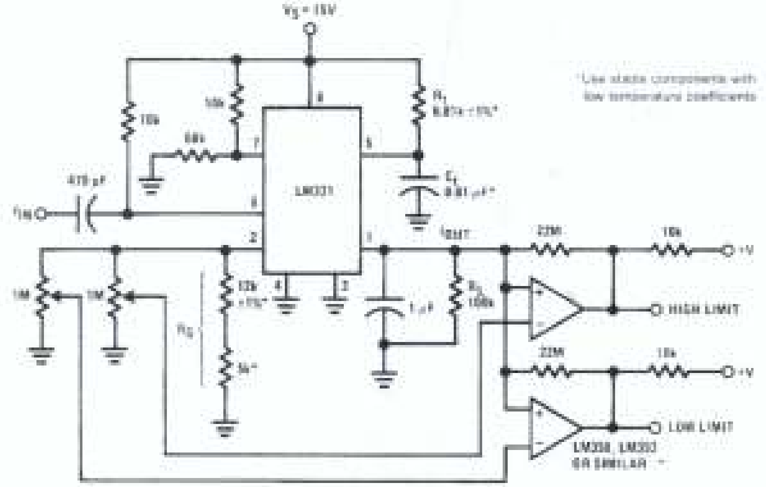
FIGURE 5. An LM334 Temperature Sensor Compensates for the F/V Circuit's Temperature Coefficient



*Use stable components with low temperature coefficients

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FIGURE 6. Combining a V/F IC with Two Comparators Produces a Slow-Response Frequency Detector

APPENDIX C

SOURCE CODE FOR THE CONTROL SOFTWARE WRITTEN IN MICROSOFT VISUAL BASIC 6.0

Declare all variables

```
Option Explicit
Dim answer, pod, TMP As Integer
Dim lagata As String
Dim calfac, start As Single
```

Codes for checks button

```
Private Sub chkmv_Click()
optk.Enabled = False
opts.Enabled = False
optj.Enabled = False
End Sub
```

Codes for Start button

```
Private Sub cmdstart_Click()
Dim IHR, IMN, ISC As Integer
Dim start As Single
IHR = Val(txtHour.Text) * 60 * 60
IMN = Val(txtmin.Text) * 60
ISC = Val(txtSec.Text)
answer = IHR + IMN + ISC
MsgBox answer
tmrsave.Enabled = True
End Sub
```

Codes for Stop button

```
Private Sub cmdstop_Click()
tmrsave.Enabled = False
End Sub
```

Codes for Directory change

```
Private Sub dirDirect_Change()
Dim lade As String
txtsad.Text = dirDirect.Path & "\Result.txt"
If drvDisk.Drive = "a:\" Then txtsad.Text = dirDirect.Path & "Result.txt"
lade = txtsad.Text
End Sub
```

Codes for Drive control

```
Private Sub drvDisk_Change()
ChDrive drvDisk.Drive
```

```
dirDirect.Path = drvDisk.Drive
End Sub
```

Codes for main form

```
Private Sub Form_Load()
start = Time
optmv.Value = True
'centering the form on the screen
Left = (Screen.Width - Width) / 2
Top = (Screen.Height - Height) / 2
ChDrive "c:"
ChDir "\odoala"
drvDisk.Drive = "c:"
dirDirect.Path = "\odoala"
'Adding item to the hour
Dim Hour As Integer
For Hour = 0 To 24
lstHour.AddItem Hour
Next Hour
'Adding item to the minute
Dim Minute As Integer
For Minute = 0 To 60
lstMin.AddItem Minute
Next Minute
'Adding item to the seconds
Dim Seconds As Integer
For Seconds = 0 To 60
lstSec.AddItem Seconds
Next Seconds
'diable save operation
tmrsave.Enabled = False
End Sub
```

Codes for data logging interval

```
Private Sub lstHour_Click()
txtHour.Text = lstHour.ListIndex
End Sub

Private Sub lstMin_Click()
txtmin.Text = lstMin.ListIndex
End Sub

Private Sub lstSec_Click()
txtSec.Text = lstSec.ListIndex
```

```
End Sub
```

Codes for Radio button

```
Private Sub optmv_Click()
optj.Enabled = False
optk.Enabled = False
opts.Enabled = False
End Sub

Private Sub optther_Click()
optj.Enabled = True
optk.Enabled = True
opts.Enabled = True
End Sub
```

Codes for Tmmer control

```
Private Sub tmrcon_Timer()
lbldate.Caption = Date$
lbltime.Caption = Time()
Dim pod, TMP As Integer
pod = ADC()
TMP = converter(pod)
If optmv.Value = True Then
lbltemp.Caption = Int(pod) & "mV"
Else
lbltemp.Caption = Int(TMP) & "C"
End If
End Sub
```

Codes for Save to file operation

```
Private Sub tmrsave_Timer()
Dim lade As String
Dim last, diff As Single
lade = txtsad.Text
last = Timer
 diff = last - start
 If diff Mod answer = 1 Then
   Open lade For Append As #1
Print #1, Time$, lbltemp.Caption
Close #1
End If
End Sub
```

Import 32.dll for hard ware control

```
'Inp and Out declarations for direct port I/O
'in 32-bit Visual Basic 4 programs.

Public Declare Function Inp Lib "inpout32.dll" _
Alias "Inp32" (ByVal PortAddress As Integer) As Integer
Public Declare Sub Out Lib "inpout32.dll" _
Alias "Out32" (ByVal PortAddress As Integer, ByVal Value As Integer)
```

Codes for the control of the ADC

```
Option Explicit

Public Function ADC() As Integer
Dim first As Integer
Dim second As Integer
Dim result As Single
Dim foward As Integer
Dim fad(5) As Integer, rel As Integer
Dim E As Integer, N As Integer, S As Integer, p As Integer
Rem READ OPERATION
Do While first = 0
  Out 890, 252
  For E = 1 To 200: Next E
  Out 890, 255
  For E = 1 To 200: Next E
  first = Inp(888)
Loop

Let S = 0
Do
  Out 890, 253
  'For E = 1 To 200: Next E
  second = Inp(888)
  S = S + 1
            If S = 200 Then
            p = 0
            Exit Do
            End If
            Loop While second = 0


 Select Case second
            Case 1: p = 256
```

```
        Case 2: p = 512
        Case 3: p = 768
        Case 4: p = 1025
        Case 5: p = 1280
        Case 6: p = 1536
        Case 7: p = 1792
        Case Else: p = 0
        End Select


ADC = first + p
End Function
```

Conversion comparison table

```
option Explicit
Dim D As Single
Dim pod As Integer

Public Function converter(ByVal pod As Integer) As Single
Select Case pod
  Case 1 To 64: Let D = 0.61
  Case 65 To 72: Let D = 0.655
  Case 73 To 79: Let D = 0.658
  Case 80 To 87: Let D = 0.669
  Case 88 To 95: Let D = 0.679
  Case 96 To 103: Let D = 0.687
  Case 104 To 111: Let D = 0.694
  Case 112 To 119: Let D = 0.7
  Case 120 To 127: Let D = 0.706
  Case 128 To 135: Let D = 0.711
  Case 136 To 144: Let D = 0.72
  Case 145 To 152: Let D = 0.724
  Case 153 To 161: Let D = 0.732
  Case 162 To 169: Let D = 0.735
  Case 170 To 178: Let D = 0.742
  Case 179 To 187: Let D = 0.748
  Case 188 To 196: Let D = 0.754
  Case 197 To 205: Let D = 0.759
  Case 206 To 214: Let D = 0.764
  Case 215 To 223: Let D = 0.769
  Case 224 To 232: Let D = 0.773
  Case 233 To 241: Let D = 0.777
  Case 242 To 250: Let D = 0.781
  Case 251 To 259: Let D = 0.785
```

Case 260 To 269: Let D = 0.791
Case 270 To 278: Let D = 0.794
Case 279 To 297: Let D = 0.803
Case 298 To 306: Let D = 0.805
Case 307 To 316: Let D = 0.81
Case 317 To 325: Let D = 0.813
Case 326 To 335: Let D = 0.817
Case 336 To 344: Let D = 0.819
Case 345 To 354: Let D = 0.823
Case 355 To 364: Let D = 0.827
Case 365 To 373: Let D = 0.829
Case 374 To 383: Let D = 0.833
Case 384 To 393: Let D = 0.836
Case 394 To 402: Let D = 0.838
Case 403 To 412: Let D = 0.841
Case 413 To 422: Let D = 0.844
Case 423 To 432: Let D = 0.847
Case 433 To 442: Let D = 0.85
Case 443 To 452: Let D = 0.853
Case 453 To 462: Let D = 0.856
Case 463 To 472: Let D = 0.858
Case 473 To 482: Let D = 0.861
Case 483 To 492: Let D = 0.863
Case 493 To 502: Let D = 0.866
Case 503 To 512: Let D = 0.868
Case 513 To 522: Let D = 0.87
Case 523 To 533: Let D = 0.874
Case 534 To 543: Let D = 0.876
Case 544 To 553: Let D = 0.878
Case 554 To 564: Let D = 0.881
Case 565 To 574: Let D = 0.883
Case 575 To 584: Let D = 0.885
Case 585 To 595: Let D = 0.888
Case 596 To 605: Let D = 0.89
Case 606 To 616: Let D = 0.893
Case 617 To 626: Let D = 0.894
Case 627 To 637: Let D = 0.897
Case 638 To 647: Let D = 0.899
Case 648 To 658: Let D = 0.901
Case 659 To 668: Let D = 0.903
Case 669 To 679: Let D = 0.905
Case 680 To 690: Let D = 0.908
Case 691 To 701: Let D = 0.91
Case 702 To 711: Let D = 0.912
Case 712 To 722: Let D = 0.914
Case 723 To 733: Let D = 0.916

```
Case 734 To 744: Let D = 0.919
Case 745 To 755: Let D = 0.921
Case 756 To 766: Let D = 0.923
Case 767 To 777: Let D = 0.925
Case 778 To 788: Let D = 0.927
Case 789 To 799: Let D = 0.929
Case 800 To 810: Let D = 0.931
Case 811 To 821: Let D = 0.933
Case 822 To 832: Let D = 0.935
Case 833 To 843: Let D = 0.937
Case 844 To 855: Let D = 0.94
Case 856 To 866: Let D = 0.941
Case 867 To 877: Let D = 0.943
Case 878 To 888: Let D = 0.945
Case 889 To 900: Let D = 0.947
Case 901 To 911: Let D = 0.949
Case 912 To 923: Let D = 0.952
Case 924 To 934: Let D = 0.953
Case 935 To 946: Let D = 0.956
Case 947 To 957: Let D = 0.957
Case 958 To 968: Let D = 0.959
Case 968 To 980: Let D = 0.961
Case 981 To 992: Let D = 0.963
Case 993 To 1004: Let D = 0.965
Case 1005 To 1015: Let D = 0.967
Case 1016 To 1027: Let D = 0.969
Case 1028 To 1039: Let D = 0.971
Case 1040 To 1051: Let D = 0.973
Case 1052 To 1062: Let D = 0.974
Case 1063 To 1074: Let D = 0.976
Case 1075 To 1086: Let D = 0.978
Case 1087 To 1098: Let D = 0.98
Case 1099 To 1110: Let D = 0.982
Case 1111 To 1122: Let D = 0.984
Case 1123 To 1134: Let D = 0.986
Case 1135 To 1146: Let D = 0.988
Case 1147 To 1158: Let D = 0.99
Case 1159 To 1170: Let D = 0.992
Case 1171 To 1182: Let D = 0.993
Case 1183 To 1194: Let D = 0.995
Case 1195 To 1206: Let D = 0.997
Case 1207 To 1218: Let D = 0.998
Case 1219 To 1230: Let D = 1
Case 1231 To 1242: Let D = 1.002
Case 1243 To 1254: Let D = 1.003
Case 1255 To 1266: Let D = 1.005
```

```
    Case 1267 To 1278: Let D = 1.006
    Case 1279 To 1290: Let D = 1.008
    Case 1291 To 1302: Let D = 1.009
    Case 1303 To 1314: Let D = 1.011
    Case 1315 To 1326: Let D = 1.012
    Case 1327 To 1338: Let D = 1.014
    Case 1339 To 1350: Let D = 1.015
    Case 1351 To 1362: Let D = 1.016
    Case 1363 To 1374: Let D = 1.018
    Case 1375 To 1386: Let D = 1.019
    Case 1387 To 1398: Let D = 1.02
    Case 1399 To 1410: Let D = 1.022
    Case 1411 To 1422: Let D = 1.023
    Case 1423 To 1434: Let D = 1.024
    Case 1435 To 1446: Let D = 1.026
    Case 1447 To 1458: Let D = 1.027
    Case 1459 To 1470: Let D = 1.028
    Case 1471 To 1482: Let D = 1.029
    Case 1483 To 1494: Let D = 1.03
    Case 1495 To 1505: Let D = 1.031
    Case 1506 To 1517: Let D = 1.032
    Case 1518 To 1529: Let D = 1.033
    Case 1530 To 1541: Let D = 1.034
    Case 1542 To 1553: Let D = 1.035
End Select
converter = pod * D
End Function
```

APPENDIX D

TC7109 12-BIT ANALOGUE-TO-DIGITAL CONVERTER APPLICATION NOTE

MICROCHIPS SEMICONDUCTOR INC

MICROCHIP

TC7109
TC7109A

12-BIT µP-Compatible Analog-To-Digital Converters

FEATURES

- **Zero-Integrator Cycle for Fast Recovery From Input Overloads**
- **Eliminates Cross -Talk in Multiplexed Systems**
- **12-Bit Plus Sign Integrating A/D Converter With Overrange Indication**
- **Sign Magnitude Coding Format**
- **True Differential Signal Input and Differential Reference Input**
- **Low Noise .... 15µV$_{P-P}$ Typ.**
- **Input Current .... 1pA Typ.**
- **No Zero Adjustment Needed**
- **TTL-Compatible, Byte-Organized Tri-State Outputs**
- **UART Handshake Mode for Simple Serial Data Transmission**

ORDERING INFORMATION

PART CODE **TC7109X**

A or blank*

Package Code	Package	Temperature Range
CKW	44-PQFP	0°C to +70°C
CLW	44-Pin PLCC	0°C to +70°C
CPL	40-Pin Plastic DIP	0°C to +70°C
IJL	40-Pin CerDIP	– 25°C to +85°C

* The "A" version has a higher I_{OUT} on the digital lines.

GENERAL DESCRIPTION

The TC7109A is a 12-bit plus sign, CMOS low-power analog-to-digital converter (ADC). Only eight passive components and a crystal are required to form a complete dual-slope integrating ADC.

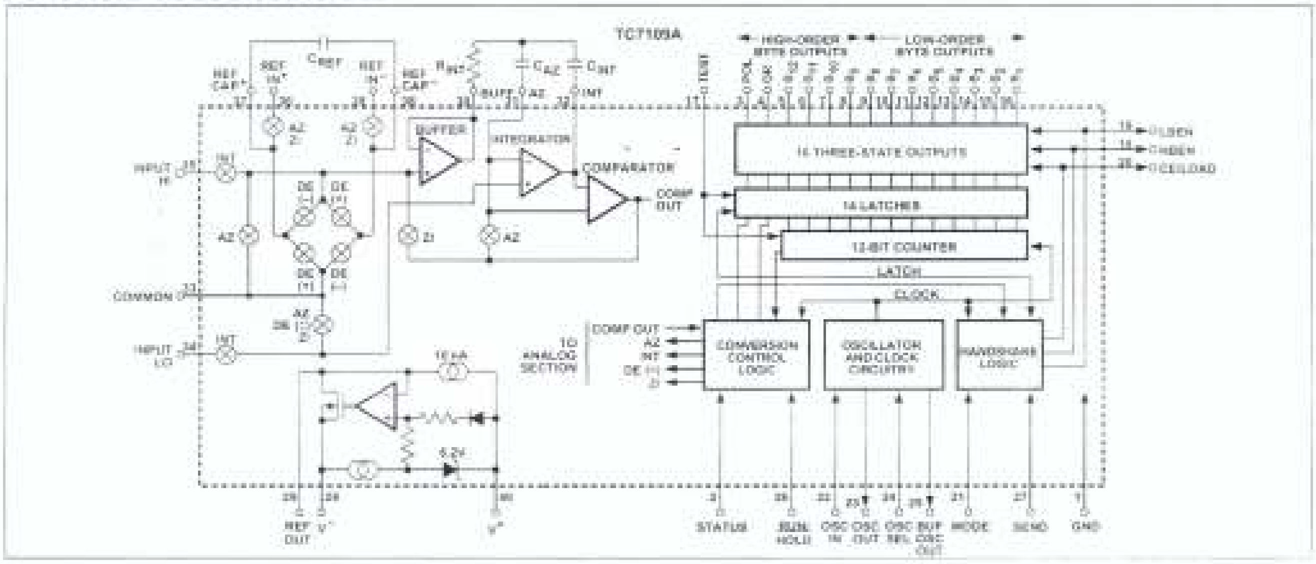
The improved V_{OH} source current TC7109A has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1pA, drift of less than 1µV/°C, input noise typically 15µV$_{P-P}$, and auto-zero. True differential input and reference allow measurement of bridge-type transducers such as load cells, strain gauges, and temperature transducers.

The TC7109A provides a versatile digital interface. In the direct mode, chip select and HIGH/LOW byte enables control parallel bus interface. In the handshake mode, the TC7109A will operate with industry-standard UARTs in controlling serial data transmission — ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/HOLD input and STATUS output.

For applications requiring more resolution, see the TC500, 15-bit plus sign ADC data sheet.

The TC7109A has improved overrange recovery performance and higher output drive capability than the original TC7109. All new (or existing) designs should specify the TC7109A wherever possible.

FUNCTIONAL BLOCK DIAGRAM



TC7109
TC7109A

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (GND to V^+)	+6.2V
Negative Supply voltage (GND to V^-)	– 9V
Analog Input Voltage (Low to High) (Note 1)	V^+ to V^-
Reference Input Voltage (Low to High (Note 1)	V^+ to V^-
Digital Input Voltage (Pins 2–27) (Note 2)	GND – 0.3V
Power Dissipation, $T_A \le 70°C$, (Note 3)	
CerDIP	2.29W
Plastic DIP	1.23W
PLCC	1.23W
PQFP	1.00W
Operating Temperature Range	
Plastic Package (C)	0°C to +70°C
Ceramic Package (I)	– 25°C to +85°C
(M)	– 55°C to +125°C
Storage Temperature Range	– 65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

NOTES:
1. Input voltages may exceed supply voltages if input current is limited to ±100µA.
2. Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latch-up. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TC7109A before its power supply is established. In multiple supply systems, the supply to the device should be activated first.
3. This limit refers to that of the package and will not occur during normal operation.

ELECTRICAL CHARACTERISTICS: All parameters with $V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = +25°C$, unless otherwise indicated.

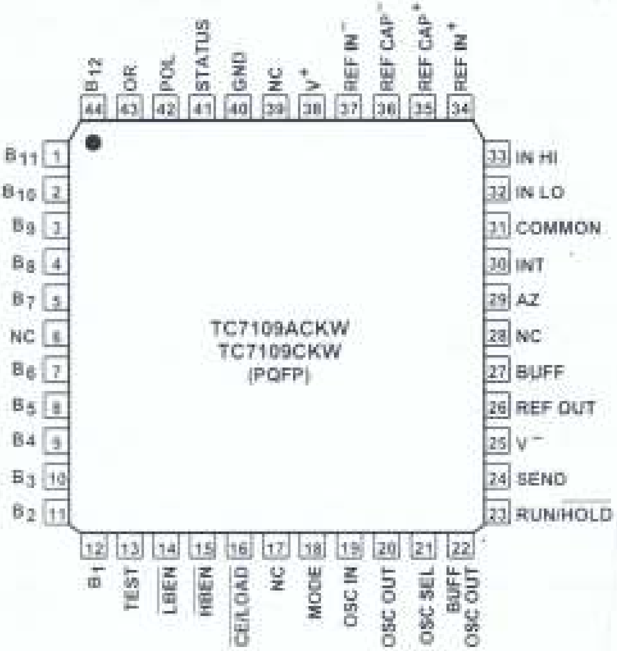
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Overload Recovery Time (TC7109A)		—	0	1	Measurement Cycle
	Zero Input Reading	$V_{IN} = 0V$ Full Scale = 409.6mV	-0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
	Ratio Metric Reading	$V_{IN} = V_{REF}$ $V_{REF} = 204.8mV$	3777_8	3777_8 4000_8	4000_8	Octal Reading
NL	Nonlinearity (Max Deviation From Best Straight Line Fit)	Full Scale = 409.6mV to 2.048V Over Full Operating Temperature Range	–1	±0.2	+1	Count
	Roll-Over Error (Difference in Reading for Equal Positive and Negative Inputs Near (Full Scale)	Full Scale = 409.6mV to 2.048V Over Full Operating Temperature Range	–1	±0.02	+1	Count
CMRR	Input Common-Mode Rejection Ratio	V_{CM} ±1V, $V_{IN} = 0V$ Full Scale = 409.6mV	—	50	—	µV/V
V_{CMR}	Common-Mode Voltage Range	Input High, Input Low, and Common Pins	$V^-+1.5$	—	V^+-1	V
e_N	Noise (P-P Value Not Exceeded 95% of Time)	$V_{IN} = 0V$ Full Scale = 409.6mV	—	15	—	µV
I_{IN}	Leakage Current at Input	V_{IN}, All Packages: +25°C C Device: $0°C \le T_A \le +70°C$ I Device: $-25°C \le T_A \le +85°C$ M Device: $-55°C \le T_A \le +125°C$	—	1 20 100 2	10 100 250 5	pA pA pA nA
TC_{ZS}	Zero Reading Drift	$V_{IN} = 0V$	—	0.2	1	µV/°C
TC_{FS}	Scale-Factor Temperature Coefficient	$V_{IN} = 408.9mV = >7770_8$ Reading, Ext Ref = 0ppm/°C	—	1	5	µV/°C
I^+	Supply Current (V^+ to GND)	$V_{IN} = 0V$, Crystal Oscillator 3.58MHz Test Circuit	—	700	1500	µA
I_S	Supply Current (V^+ to V^-)	Pins 2–21, 25, 26, 27, 29 Open	—	700	1500	µA

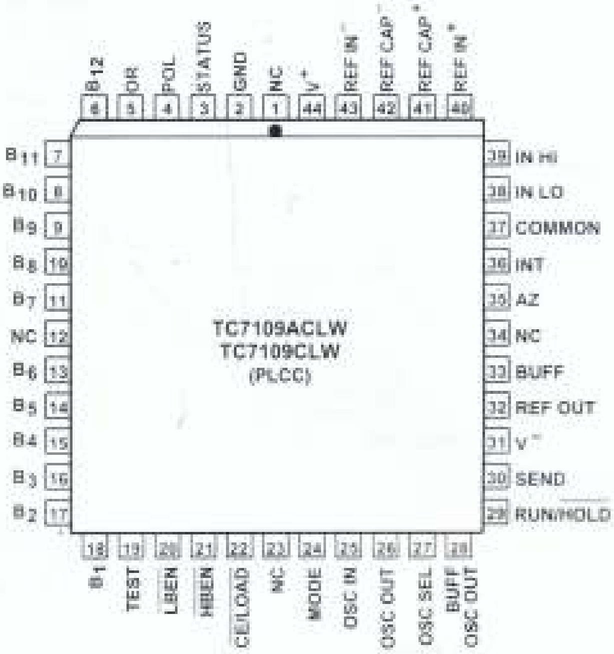
ELECTRICAL CHARACTERISTICS (Cont.)

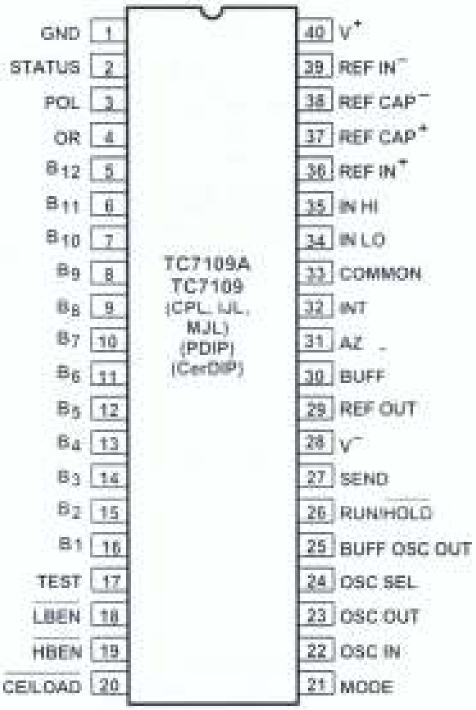
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{REF}	Ref Out Voltage	Referenced to V^+, 25kΩ Between V^+ and Ref Out	−2.4	−2.8	−3.2	V
TC_{REF}	Ref Out Temperature Coefficient	25kΩ Between V^+ and Ref Out $0°C \le T_A \le +70°C$	—	80	—	ppm/°C
Digital						
V_{OH}	Output High Voltage TC7109A: I_{OUT} = 700µA	TC7109: I_{OUT} = 100µA Pins 3 – 16, 18, 19, 20	3.5	4.3	—	V
V_{OL}	Output Low Voltage	I_{OUT} = 1.6mA	—	0.2	0.4	V
	Output Leakage Current	Pins 3 – 16 High Impedance	—	±0.01	±1	µA
	Control I/O Pull-Up Current	Pins 18, 19, 20 $V_{OUT} = V^+ - 3V$ Mode Input at GND	—	5	—	µA
	Control I/O Loading	HBEN, Pin 19; $\overline{\text{LBEN}}$, Pin 18	—	—	50	pF
V_{IH}	Input High Voltage	Pins 18 – 21, 26, 27 Referenced to GND	2.5	—	—	V
V_{IL}	Input Low Voltage	Pins 18 – 21, 26, 27 Referenced to GND	—	—	1	V
	Input Pull-Up Current	Pins 26, 27; $V_{OUT} = V^+ - 3V$ Pins 17, 24; $V_{OUT} = V^+ - 3V$	—	5 25	—	µA µA
	Input Pull-Down Current	Pin 21; V_{OUT} = GND + +3V	—	1	—	µA
	Oscillator Output Current, High	V_{OUT} = 2.5V	—	1	—	mA
	Oscillator Output Current, Low	V_{OUT} = 2.5V	—	1.5	—	mA
	Buffered Oscillator Output Current, High	V_{OUT} = 2.5V	—	2	—	mA
	Buffered Oscillator Output Current, Low	V_{OUT} = 2.5V	—	5	—	mA
t_W	Mode Input Pulse Width		60	—	—	nsec

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, antistatic tubes, or other conducting material. Use proper antistatic handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

PIN CONFIGURATIONS







NC = NO INTERNAL CONNECTION

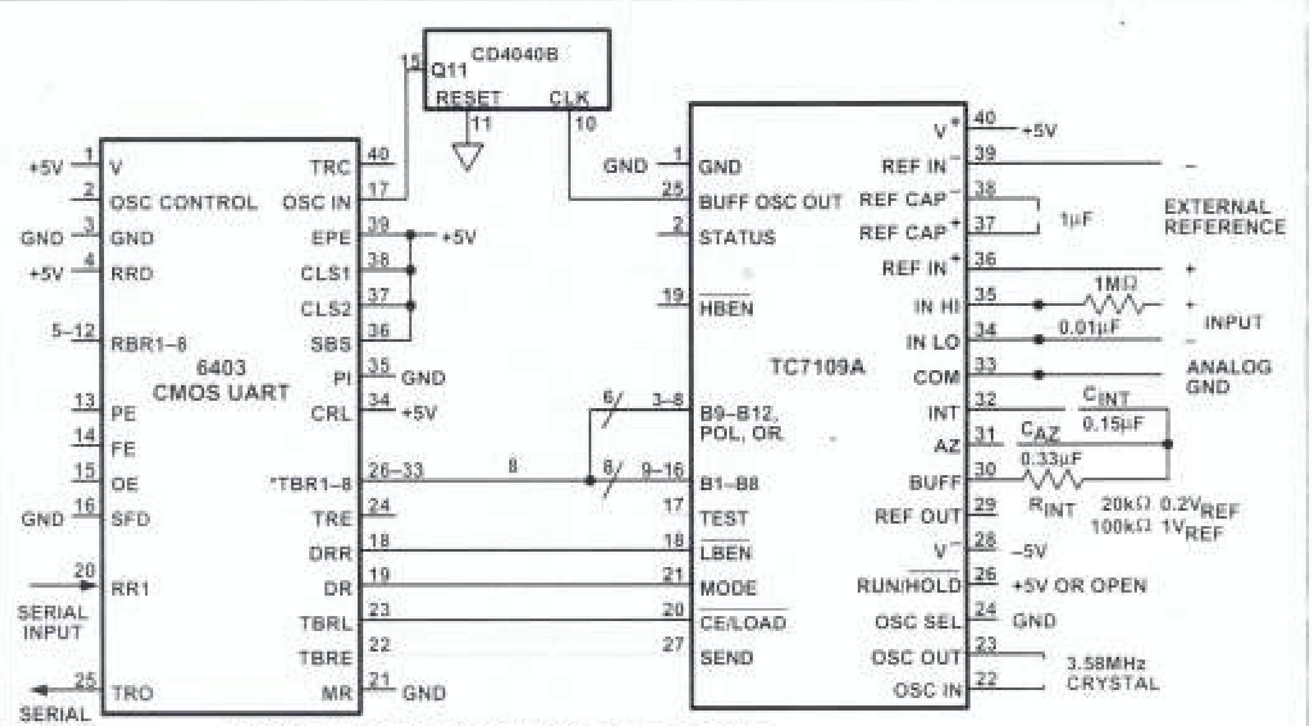
TC7109/A PIN DESCRIPTION

Pin No. (40-Pin PDIP)	Symbol	Description	
1	GND	Digital ground, 0V, ground return for all digital logic.	
2	STATUS	Output HIGH during integrate and deintegrate until data is latched. Output LOW when analog section is in auto-zero or zero-integrator configuration.	
3	POL	Polarity — High for positive input.	
4	OR	Overrange — High if overranged.	All Three-State Data Bits
5	B_{12}	Bit 12 (Most Significant Bit)	
6	B_{11}	Bit 11	
7	B_{10}	Bit 10	
8	B_9	Bit 9	
9	B_8	Bit 8	
10	B_7	Bit 7	
11	B_6	Bit 6	
12	B_5	Bit 5	
13	B_4	Bit 4	
14	B_3	Bit 3	
15	B_2	Bit 2	
16	B_1	Bit 1 (Least Significant Bit)	
17	TEST	Input High — Normal operation. Input LOW — Forces all bit outputs HIGH. **Note:** This input is used for test purposes only.	
18	$\overline{\text{LBEN}}$	Low-Byte Enable — With MODE (Pin 21) LOW, and $\overline{\text{CE/LOAD}}$ (Pin 20) LOW, taking this pin LOW activates low-order byte outputs, B1–B8. With MODE (Pin 21) HIGH, this pin serves as low-byte flag output used in handshake mode. See Figures 7, 8, and 9.	
19	$\overline{\text{HBEN}}$	High-Byte Enable — With MODE (Pin 21) LOW, and $\overline{\text{CE/LOAD}}$ (Pin 20) LOW, taking this pin LOW activates high-order byte outputs, B9–B12, POL, OR. With MODE (Pin 21) HIGH, this pin serves as high-byte flag output used in handshake mode. See Figures 7, 8, and 9.	
20	$\overline{\text{CE/LOAD}}$	Chip Enable/Load — With MODE (Pin 21) LOW, $\overline{\text{CE/LOAD}}$ serves as a master output enable. When HIGH, B1–B12, POL, OR outputs are disabled. When MODE (Pin 21) is HIGH, a load strobe is used in handshake mode. See Figure 7, 8, and 9.	
21	MODE	Input LOW — Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and LBEN (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed HIGH — Causes immediate entry into handshake mode and output of data as in Figure 9. Input HIGH — Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversions completion.	
22	OSC IN	Oscillator Input.	
23	OSC OUT	Oscillator Output.	
24	OSC SEL	Oscillator Select — Input HIGH configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. Input LOW configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.	
25	BUF OSC OUT	Buffered Oscillator Output.	
26	$\overline{\text{RUN/HOLD}}$	Input HIGH — Conversions continuously performed every 8192 clock pulses. Input LOW — Conversion in progress completed; converter will stop in auto-zero seven counts before integrate.	

TC7109/A PIN DESCRIPTION (Cont.)

Pin No. (40-Pin PDIP)	Symbol	Description
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to V^+ if not used.
28	V^-	Analog Negative Supply — Nominally – 5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally 2.8V down from V^+ (Pin 40).
30	BUFFER	Buffer Amplifier Output.
31	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}.
32	INTEGRATOR	Integrator Output — Outside foil of C_{INT}.
33	COMMON	Analog Common — System is auto-zeroed to COMMON.
34	INPUT LOW	Differential Input Low Side.
35	INPUT HIGH	Differential Input High Side.
36	REF IN^+	Differential Reference Input Positive.
37	REF CAP^+	Reference Capacitor Positive.
38	REF CAP^-	Reference Capacitor Negative.
39	REF IN^-	Differential Reference Input Negative.
40	V^+	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.



*NOTE: For lowest power consumption, TBR1–TBR8 inputs should have 100kΩ pull-up resistors to +5V.

Figure 1. TC7109A UART Interface (Send Any Word to UART to Transmit Latest Result)

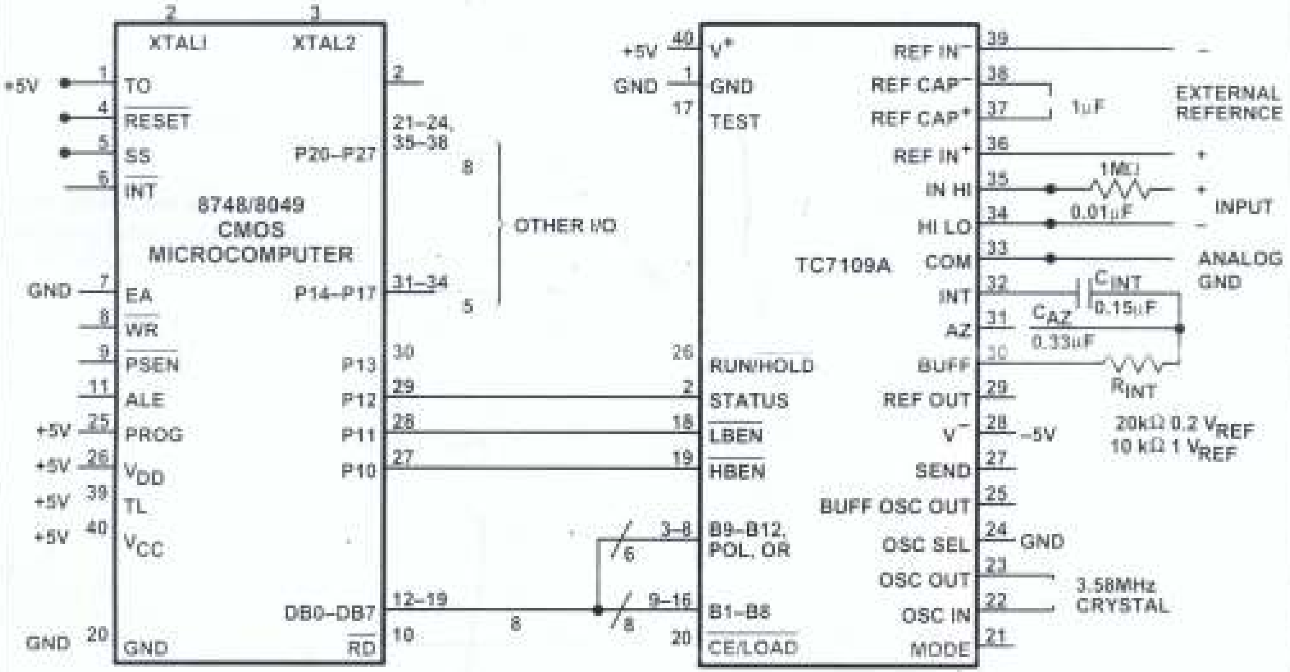


Figure 2. TC7109A Parallel Interface With 8048/8049 Microcomputer

DETAILED DESCRIPTION

(All Pin Designations Refer to 40-Pin DIP)

Analog Section

The functional diagram shows a block diagram of the analog section of the TC7109A. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/HOLD input is left open or connected to V⁺. Each measurement cycle is divided into four phases, as shown in Figure 3. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE), and (4) Zero Integrator (ZI).

Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. The offset referred to the input is less than 10µV.

Signal-Integrate Phase

The buffer and integrator inputs are removed from common and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter's power supply, input low can be tied to analog common to establish the correct common-mode voltage.

Deintegrate Phase

Input high is connected across the previously-charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by auto-zero) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Zero-Integrator Phase

The ZI phase only occurs when an input overrange condition exists. The function of the ZI phase is to eliminate residual charge on the integrator capacitor after an overrange measurement. Unless removed, the residual charge will be transferred to the auto-zero capacitor and cause an error in the succeeding conversion.

The ZI phase virtually eliminates hysteresis or "cross talk" in multiplexed systems. An overrange input on one channel will not cause an error on the next channel measured. This feature is especially useful in thermocouple measurements, where unused (or broken thermocouple) inputs are pulled to the positive supply rail.

During ZI, the reference capacitor is charged to the reference voltage. The signal inputs are disconnected from the buffer and integrator. The comparator output is connected to the buffer input, causing the integrator output to be driven rapidly to 0V (Figure 3). The ZI phase only occurs following an overrange and lasts for a maximum of 1024 clock periods.

Differential Input

The TC7109A has been optimized for operation with analog common near digital ground. With +5V and –5V power supplies, a full ±4V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86dB is achieved for input differential voltages anywhere within the typical common-mode range of 1V below the positive supply to 1.5V above the negative supply. However, for optimum performance, the IN HI and IN LO inputs should not come within 2V of either supply rail. Since the integrator also swings with the common-mode voltage, care must be exercised to ensure the integrator output does not saturate. A worst-case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Roll-over voltage is the main source of common-mode error, caused by the reference capacitor losing or gaining charge due to stray capacity on its nodes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to deintegrate a positive signal and lose charge (decrease voltage) when called upon to deintegrate a negative input signal. This difference in reference for (+) or (–) input voltages will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparison to the stray capacitance. To minimize roll-over error from these sources, keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in the block diagram (Figure 4) and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL compatible three-state output drivers, UART handshake logic, polarity, overrange, and control logic. Logic levels are referred to as LOW or HIGH.

Inputs driven from TTL gates should have 3kΩ to 5kΩ pull-up resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (LOW) to V^+ (HIGH).

STATUS Output

During a conversion cycle, the STATUS output goes HIGH at the beginning of signal integrate and goes LOW one-half clock period after new data from the conversion has been stored in the output latches (see Figure 3). The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while status is LOW.)

MODE Input

The output mode of the converter is controlled by the MODE input. The converter is in its "direct" output mode, when the MODE input is LOW or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pull-down resistor to ensure a LOW Level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in 2 bytes, then returns to "direct" mode. When the MODE input is kept HIGH, the converter will output data in the handshake mode at the end of every conversion cycle. With MODE = 0 (direct bus transfer), the send input should be tied to V^+. (See "Handshake Mode.")

RUN/$\overline{\text{HOLD}}$ Input

With the RUN/$\overline{\text{HOLD}}$ input high, or open, the circuit operates normally as a dual-slope ADC, as shown in Figure 3. Conversion cycles operate continuously with the output latches updated after zero crossing in the deintegrate mode. An internal pull-up resistor is provided to ensure a HIGH level with an open input.

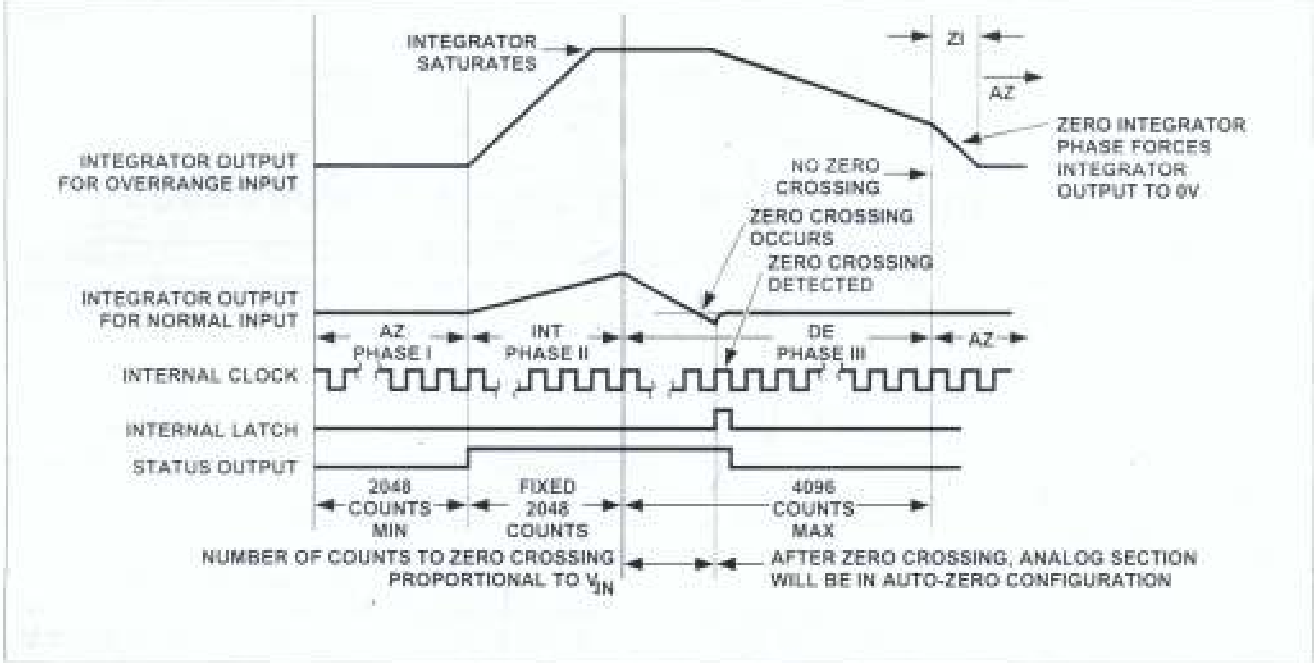


Figure 3. Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

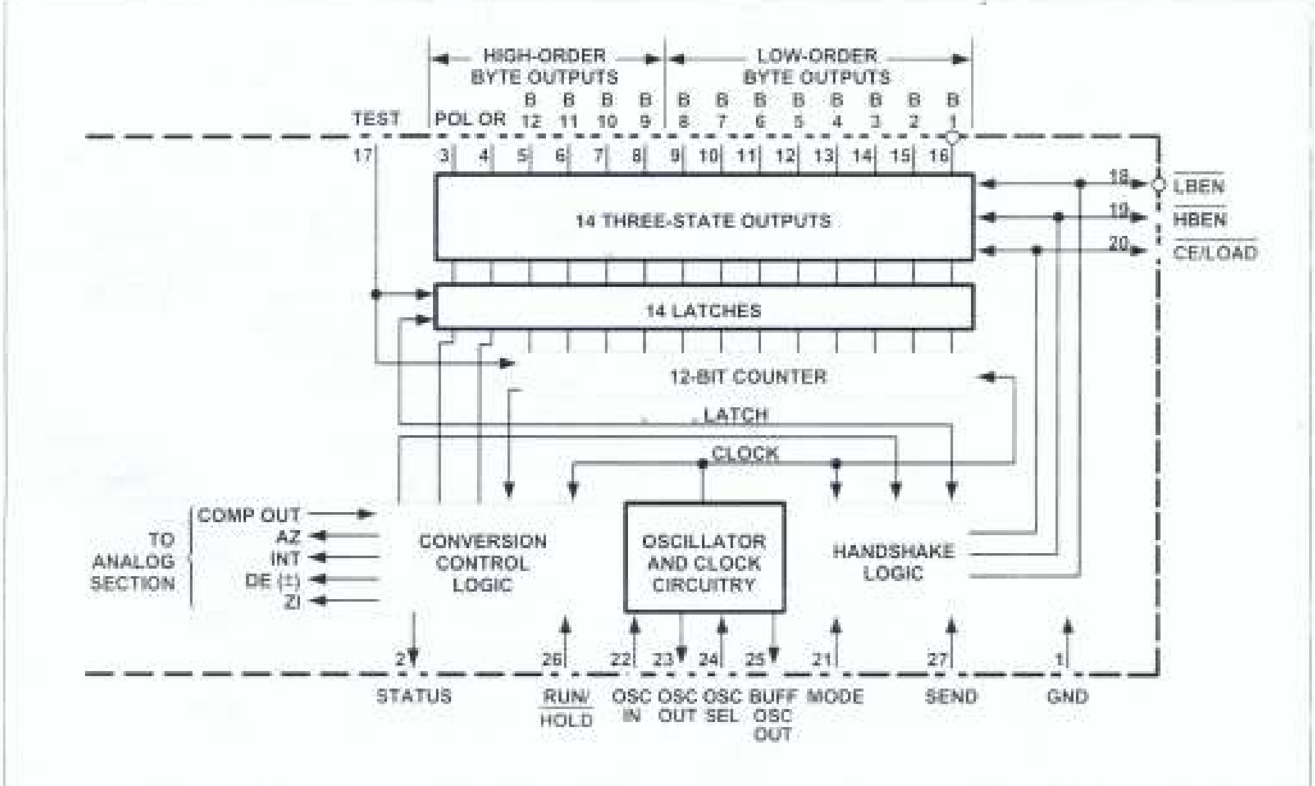
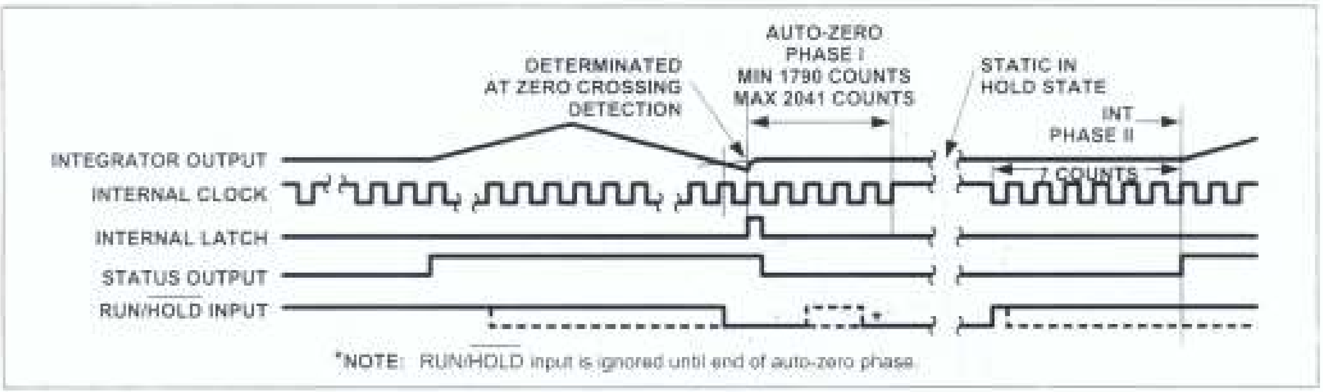


Figure 4. Digital Section



*NOTE: RUN/$\overline{\text{HOLD}}$ input is ignored until end of auto-zero phase.

Figure 5. TC7109A RUN/$\overline{\text{HOLD}}$ Operation

The RUN/$\overline{\text{HOLD}}$ input may be used to shorten conversion time. If RUN/$\overline{\text{HOLD}}$ goes LOW any time after zero crossing in the deintegrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in deintegrate.

If RUN/$\overline{\text{HOLD}}$ stays or goes LOW, the conversion will complete with minimum time in deintegrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a HIGH at the RUN/$\overline{\text{HOLD}}$ input. As shown in Figure 5, the STATUS output will go HIGH 7 clock periods after RUN/$\overline{\text{HOLD}}$ is changed to HIGH, and the converter will begin the integrate phase of the next conversion.

The RUN/$\overline{\text{HOLD}}$ input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ LOW. The conversion is started when RUN/$\overline{\text{HOLD}}$ goes HIGH, and the new data is valid when the STATUS output goes LOW (or is transferred to the UART; see "Handshake Mode"). RUN/$\overline{\text{HOLD}}$ may now go LOW, terminating deintegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/$\overline{\text{HOLD}}$ goes LOW during deintegrate, after zero crossing, and goes HIGH after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the buffered oscillator output. In this mode, the input value measured determines the conversion time.

Direct Mode

The data outputs (bits 1 through 8, low-order bytes; bits 9 through 12, polarity and overrange high-order bytes) are accessible under control of the byte and chip enable terminals as inputs with the MODE pin at a LOW level. These three inputs are all active LOW. Internal pull-up resistors are provided for an inactive HIGH level when left open. When chip enable is LOW, a byte-enable input LOW will allow the outputs of the byte to become active. A variety of parallel data accessing techniques may be used, as shown in the "Interfacing" section. (See Figure 6 and Table 1.)

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output. This prevents accessing data while it is being updated and eliminates the acquisition of erroneous data.

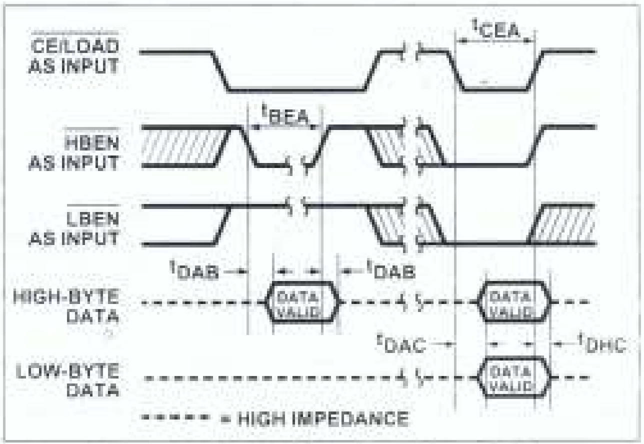


Figure 6. TC7109A Direct Mode Output Timing

Table 1. TC7109A Direct Mode Timing Requirements

Symbol	Description	Min	Typ	Max	Units
t_{BEA}	Byte Enable Width	200	500		nsec
t_{DAB}	Data Access Time From Byte Enable		150	300	nsec
t_{DHB}	Data Hold Time From Byte Enable		150	300	nsec
t_{CEA}	Chip Enable Width	300	500		nsec
t_{DAC}	Data Access Time From Chip Enable		200	400	nsec
t_{DHC}	Data Hold Time From Chip Enable		200	400	nsec

Handshake Mode

An alternative means of interfacing the TC7109A to digital systems is provided when the handshake output mode of the TC7109A becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TC7109A and industry-standard UARTs with no external logic required. The TC7109A provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

The MODE input controls the handshake mode. When the MODE input is held HIGH, the TC7109A enters the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figures 7 and 8). Entry into the handshake mode may be triggered on demand by the MODE input. At any time during the conversion cycle, the LOW-to-HIGH transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. The MODE input is ignored in the handshake mode, and until the converter completes the output cycle and clears the handshake mode, data updating will be inhibited (see Figure 9).

When the MODE input is HIGH or when the converter enters the handshake mode, the chip and byte enable inputs become TTL-compatible outputs which provide the output cycle control signals (see Figures 7, 8 and 9).

The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the handshake mode. The sequence of the output cycle with SEND held HIGH is shown in Figure 7. The handshake mode (internal MODE HIGH) is entered after the data latch pulse (the CE/LOAD, LBEN and HBEN terminals are active as outputs since MODE remains HIGH).

The HIGH level at the SEND input is sensed on the same HIGH-to-LOW internal clock edge. On the next LOW-to-HIGH internal clock edge, the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled and the CE/LOAD and the HBEN outputs assume a LOW level. The CE/LOAD output remains LOW for one full internal clock period only; the data outputs remain active for 1-1/2 internal clock periods; and the high-byte enable remains LOW for 2 clock periods. The CE/LOAD output LOW level or LOW-to-HIGH edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining HIGH the converter completes the output cycle using CE/LOAD and LBEN while the low-order byte outputs (bits 1 through 8) are activated. When both bytes are sent, the handshake mode is terminated. The typical UART interfacing timing is shown in Figure 8. The SEND input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows an industry-standard HD6403 or CDP1854 CMOS UART to interface to serial data channels. The SEND input to the TC7109A is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the CE/LOAD input of the TC7109A drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter buffer register inputs accept the parallel data outputs. With the UART transmitter buffer register empty, the SEND input will be HIGH when the handshake mode is entered after new data is stored. The high-order byte outputs become active and the CE/LOAD and HBEN inputs will go LOW after SEND is sensed. When CE/LOAD goes HIGH at the end of one clock period, the high-order byte data is clocked into the UART transmitter buffer register. The UART TBRE output will go LOW, which halts the output cycle with the HBEN output LOW, and the high-order byte outputs active. When the UART has transferred the data to the transmitter register and cleared the transmitter buffer register, the TBRE returns HIGH. The high-order byte outputs are disabled on the next TC7109A internal clock HIGH-to-LOW edge, and one-half internal clock later, the HBEN output returns HIGH. The CE/LOAD and LBEN outputs go LOW at the same time as the low-order byte outputs become active. When the CE/LOAD returns HIGH at the end of one clock period, the low-order data is clocked into the UART transmitter buffer register, and TBRE again goes LOW. The next TC7109A internal clock HIGH-to-LOW edge will sense when TBRE returns to a HIGH, disabling the data inputs. One-half internal clock later, the handshake mode is cleared, and the CE/LOAD, HBEN and LBEN terminals return HIGH and stay active, if MODE still remains HIGH.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a LOW-to-HIGH edge on the MODE input. A handshake output sequence triggered is shown in Figure 9. The SEND input is LOW when the converter enters handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

Figure 9 also shows that the output sequence can take longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

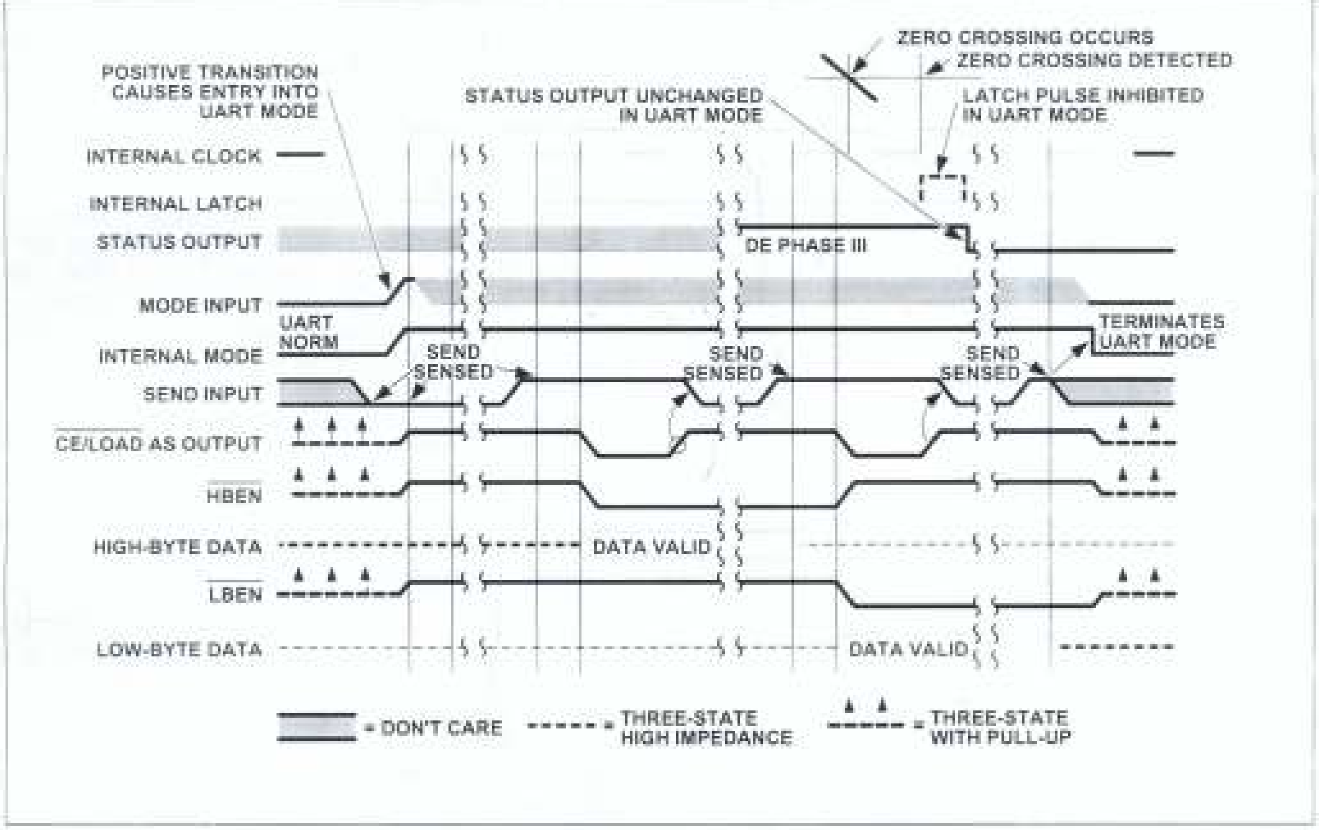


Figure 9. TC7109A Handshake Triggered by MODE Input

Oscillator

The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pull-up resistor. When the OSCILLATOR SELECT input is HIGH or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure 10. The circuit will oscillate at a frequency given by f = 0.45/RC. A 100kΩ resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60Hz period for optimum 60Hz line rejection.

With OSCILLATOR SELECT input LOW, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1MHz to 5MHz range with no external components (Figure 11). The OSCILLATOR SELECT input LOW inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58MHz TV crystal gives a division ratio providing an integration time given by:

$$t = (2048\ \text{clock periods})\ \frac{58}{3.58\text{MHz}} = 33.18\text{msec}$$

The error is less than 1% from two 60Hz periods, or 33.33msec, which will give better than 40dB, 60Hz rejection. The converter will operate reliably at conversion rates up to 30 per second, corresponding to a clock frequency of 245.8kHz.

When the oscillator is to be overdriven, the OSCILLATOR OUTPUT should be left open, and the overdriving signal should be applied at the OSCILLATOR INPUT. The internal clock will be of the same duty cycle, frequency and phase as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

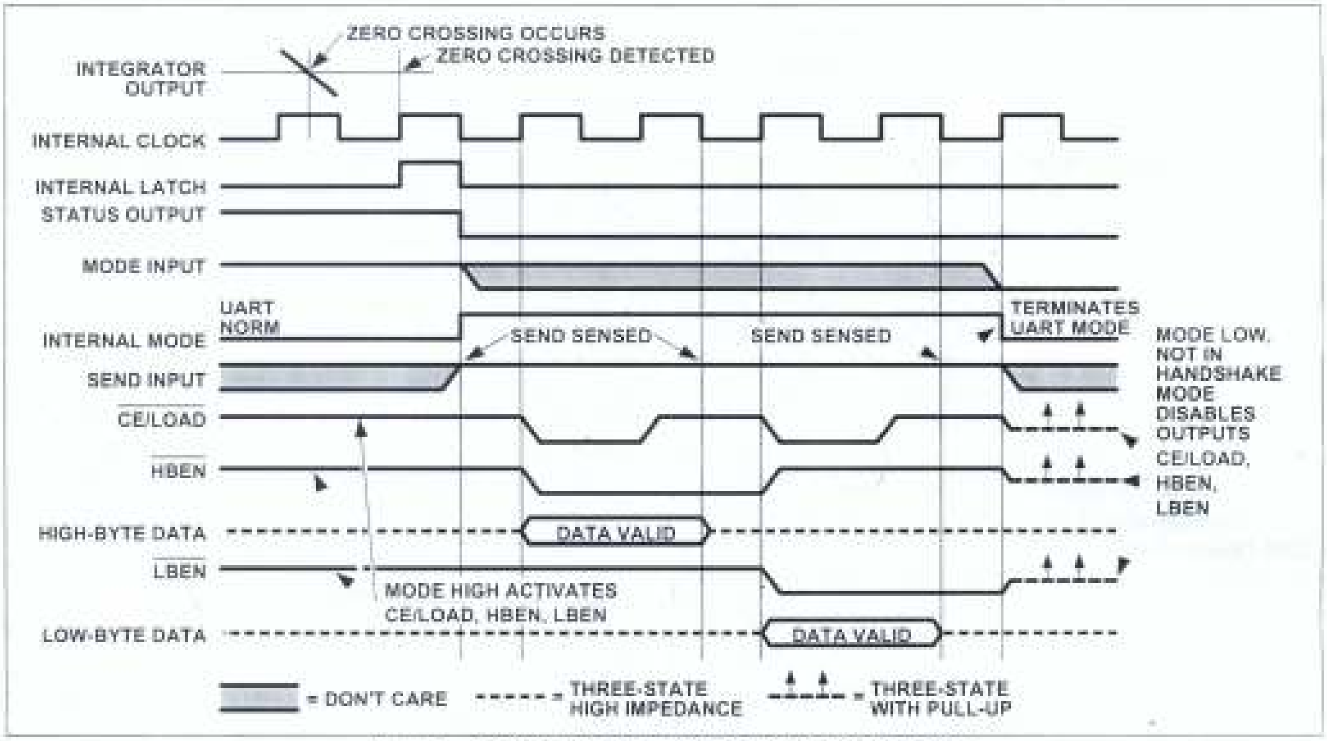


Figure 7. TC7109A Handshake With SEND INPUT Held Positive

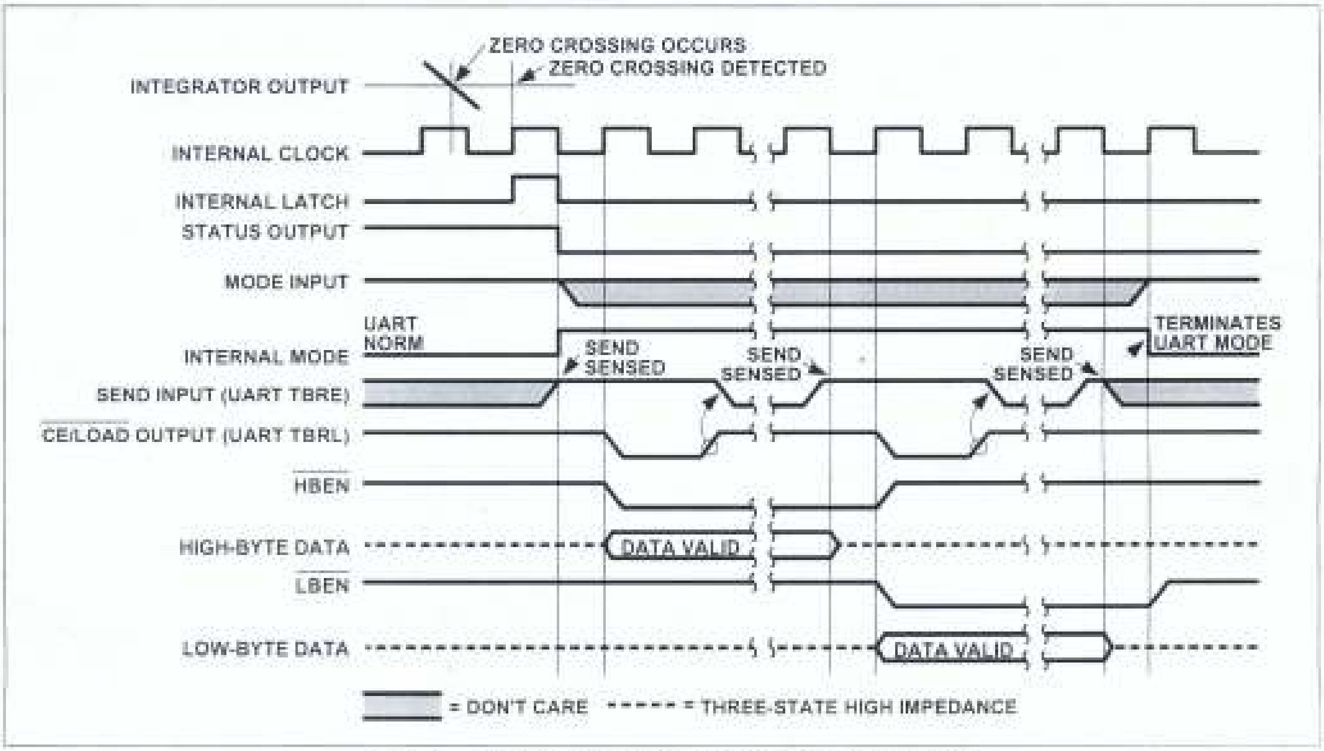


Figure 8. TC7109A Handshake — Typical UART Interface Timing

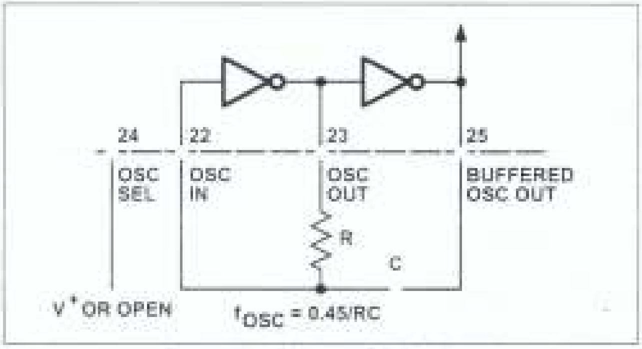


Figure 10. TC7109A RC Oscillator

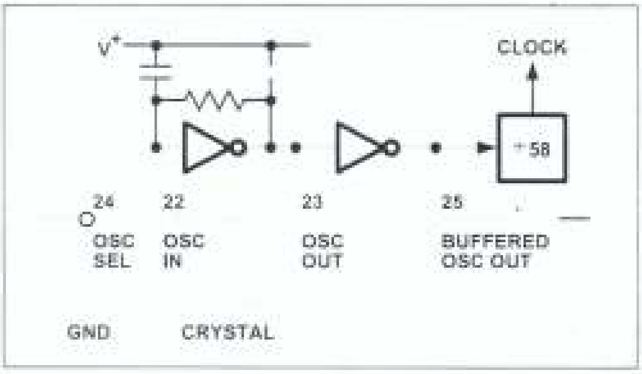


Figure 11. TC7109A Crystal Oscillator

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled and the counter outputs are all forced into the HIGH state. When the input returns to the 1/2 (V^+ – GND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the LOW state.

The counter output latches are enabled when the TEST input is taken to a level halfway between V^+ and GND, allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full-scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly effecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common-mode voltage range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and roll-over errors will be slightly worse than in the ±4V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and roll-over errors. To improve performance, ±6V supplies may be used.

Integrating Capacitor

The integrating capacitor, C_{INT}, should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3V from either supply. A ±3.5V to ±4V integrator output swing is nominal for the TC7109A, with ±5V supplies and analog common connected to GND. For 7-1/2 conversions per second (61.72 kHz internal clock frequency), nominal values C_{INT} and C_{AZ} are 0.15µF and 0.33µF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\,(20\mu A)}{\text{Integrator Output Voltage Swing}}$$

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors give undetectable errors, at reasonable cost, up to +85°C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat between units, devices may be selected to less than 0.5 count of error due to dielectric absorption.

Integrating Resistor

The integrator and buffer amplifiers have a class A output stage with 100µA of quiescent current. They supply 20µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2.048V full-scale a 100kΩ resistor is recommended and for 409.6mV full-scale a 20k resistor is recommended. R_{INT} may be selected for other values of full scale by:

$$R_{INT} = \frac{\text{Full-Scale Voltage}}{20\mu A}$$

Auto-Zero Capacitor

As the auto-zero capacitor is made large, the system noise is reduced. Since the TC7109A incorporates a zero integrator cycle, the size of the auto-zero capacitor does not affect overload recovery. The optimal value of the auto-zero capacitor is between 2 and 4 times C_{INT}. A typical value for C_{AZ} is 0.33µF.

Direct interfacing to most microprocessor busses is easily accomplished through the three-state output of the TC7109A.

Figures 1, 17 and 18 are typical connection diagrams. To ensure requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low, providing simple address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

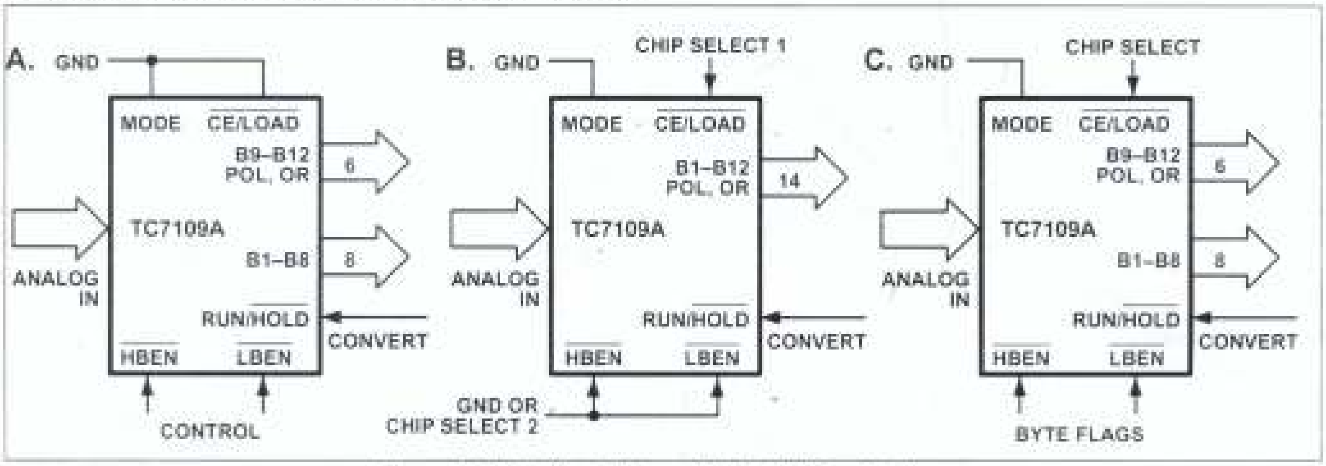


Figure 12. Direct Mode Chip and Byte Enable Combinations

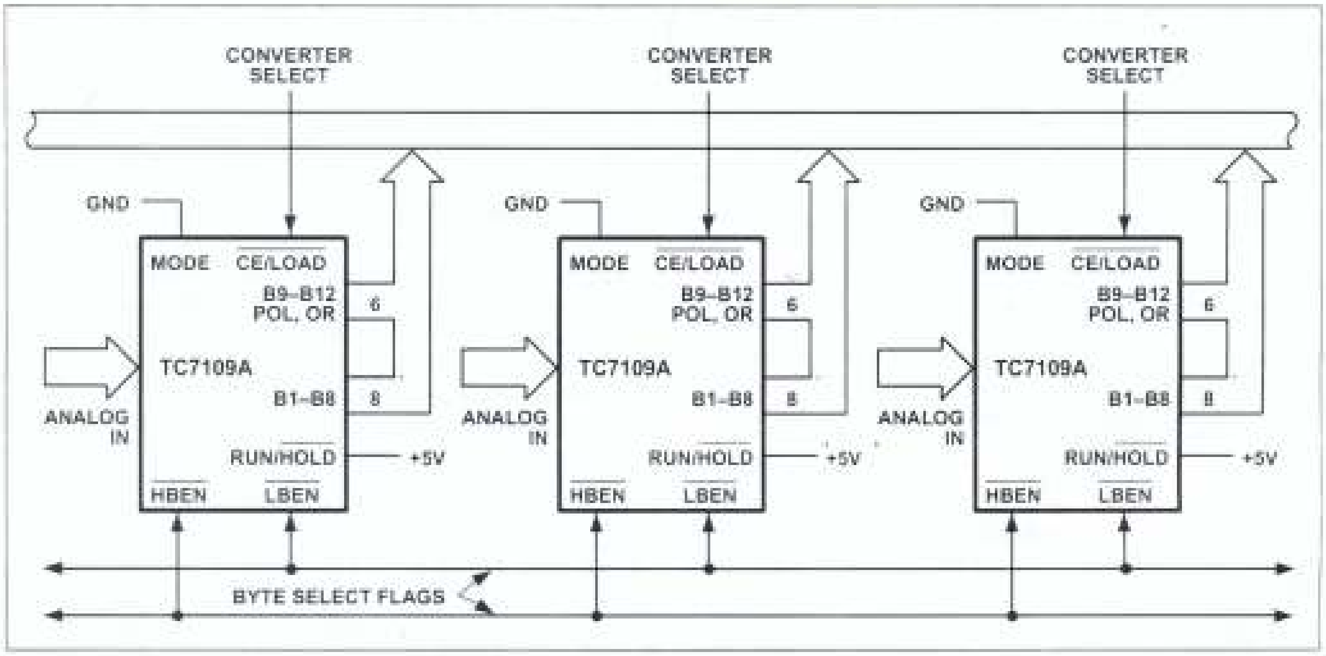


Figure 13. Three-Stating Several TC7109A's to a Small Bus

The inner foil of C_{AZ} should be connected to pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to pin 32 for best rejection of stray pickups. For low leakage at temperatures above +85°C, use Teflon capacitors.

Reference Capacitor

A 1μF capacitor is recommended for most circuits. However, where a large common-mode voltage exists, a larger value is required to prevent roll-over error (e.g., the reference low is not analog common), and a 409.6mV scale is used. The roll-over error will be held to 0.5 count with a 10μF capacitor. For temperatures above +80°C use Teflon or equivalent capacitors for their low leakage characteristics.

Reference Voltage

To generate full-scale output of 4096 counts, the analog input required is $V_{IN} = 2\ V_{REF}$. For 409.6mV full scale, use a reference of 204.8mV. In many applications, where the ADC is connected to a transducer, a scale factor will exist between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage for the transducer is 700mV. Instead of dividing the input down to 409.6mV, the designer should use the input voltage directly and select V_{REF} = 350mV. Suitable values for integrating resistor and capacitor would be 34kΩ and 0.15μF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements with an offset or tare are desired for nonzero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor-based systems using the TC7109A, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

Reference Sources

A major factor in the absolute accuracy of the ADC is the stability of the reference voltage. The 12-bit resolution of the TC7109A is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 70ppm/°C, a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled, or where high-accuracy absolute measurements are being made, it is recommended that an external high-quality reference be used.

A reference output (pin 29) is provided which may be used with a resistive divider to generate a suitable reference voltage (20mA may be sunk without significant variation in output voltage). A pull-up bias device is provided which sources about 10μA. The output voltage is nominally 2.8V below V^+. When using the on-board reference, REF OUT (pin 29) should be connected to REF^- (pin 39), and REF^+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+. The test circuit shows the circuit for a 204.8mV reference, generated by a 2kΩ precision potentiometer in series with a 24kΩ fixed resistor.

Interfacing

Direct Mode

Combinations of chip-enable and byte-enable control signals which may be used when interfacing the TC7109A to parallel data lines are shown in Figure 12. The CE/LOAD input may be tied low, allowing either byte to be controlled by its own enable (Figure 12A). Figure 12B shows the HBEN and LBEN as flag inputs, and CE/LOAD as a master enable, which could be the READ strobe available from most microprocessors. Figure 12C shows a configuration where the two byte enables are connected together. The CE/LOAD is a chip enable, and the HBEN and LBEN may be used as a second chip enable, or connected to ground. The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V^+.

Figure 13 shows interfacing several TC7109A's to a bus, ganging the HBEN and LBEN signals to several converters together, and using the CE/LOAD input to select the desired converter.

Figures 14 – 19 give practical circuits utilizing the parallel three-state output capabilities of the TC7109A. Figure 14 shows parallel interface to the Intel MCS-48, -80 and -85 systems via an 8255 PPI, where the TC7109A data outputs are active at all times. The 8155 I/O ports may be used in an identical manner. This interface can be used in a read-after-update sequence, as shown in Figure 15. The data is accessed by the high-to-low transition of the STATUS driving an interrupt to the microprocessor.

The RUN/HOLD input is also used to initiate conversions under software control. Figure 16 gives an interface to Motorola MC6800 or MOS Technology MCS650X system.

An interrupt is generated through the Control Register B, CB1 line from the high-to-low transition of the STATUS output. The RUN/HOLD pin is controlled by CB2 through Control Register B, allowing software control of conversions.

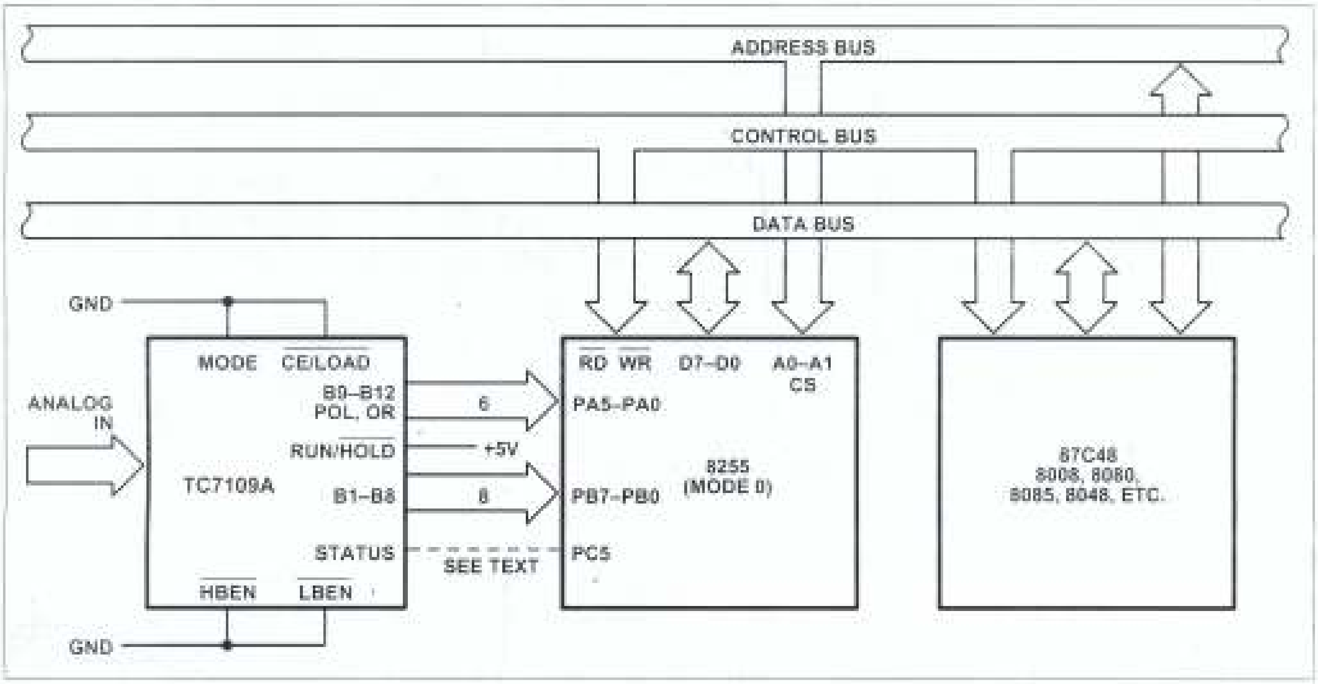


Figure 14. Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers

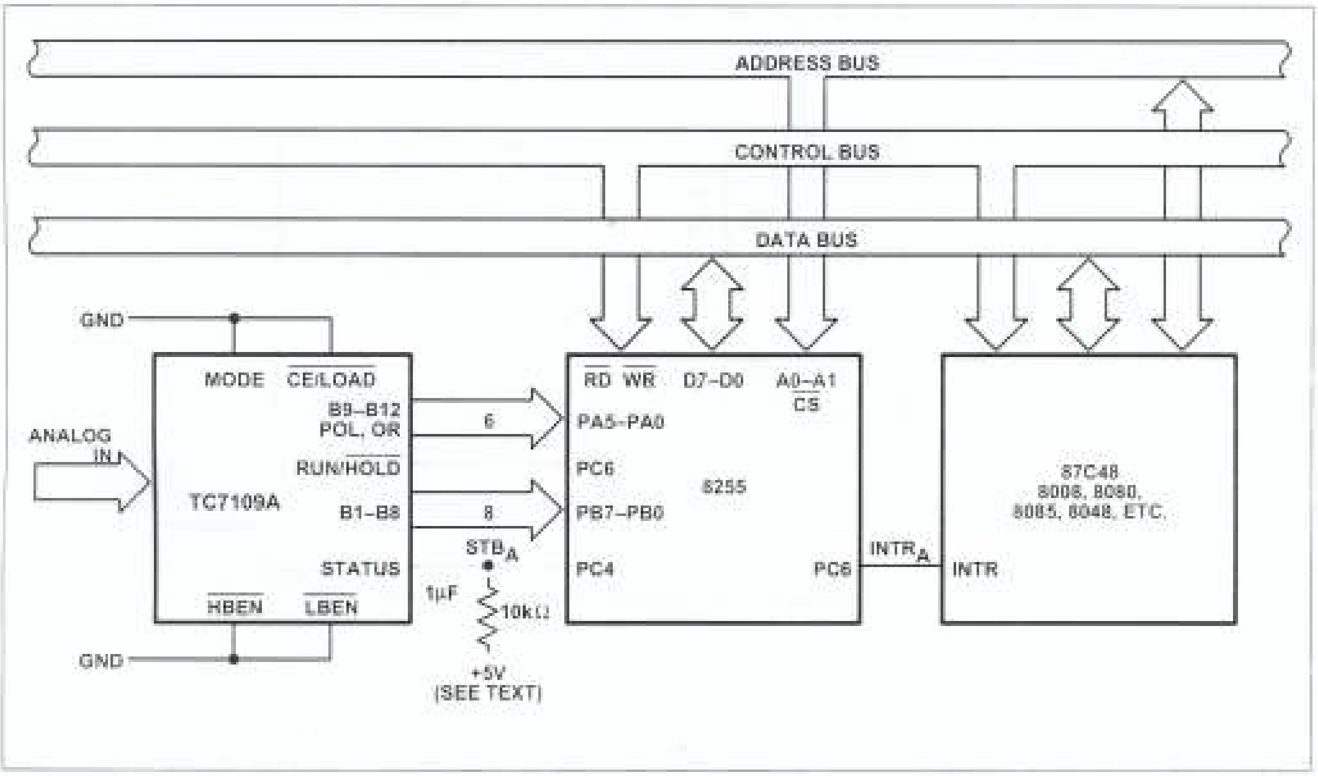


Figure 15. Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers With Interrupt

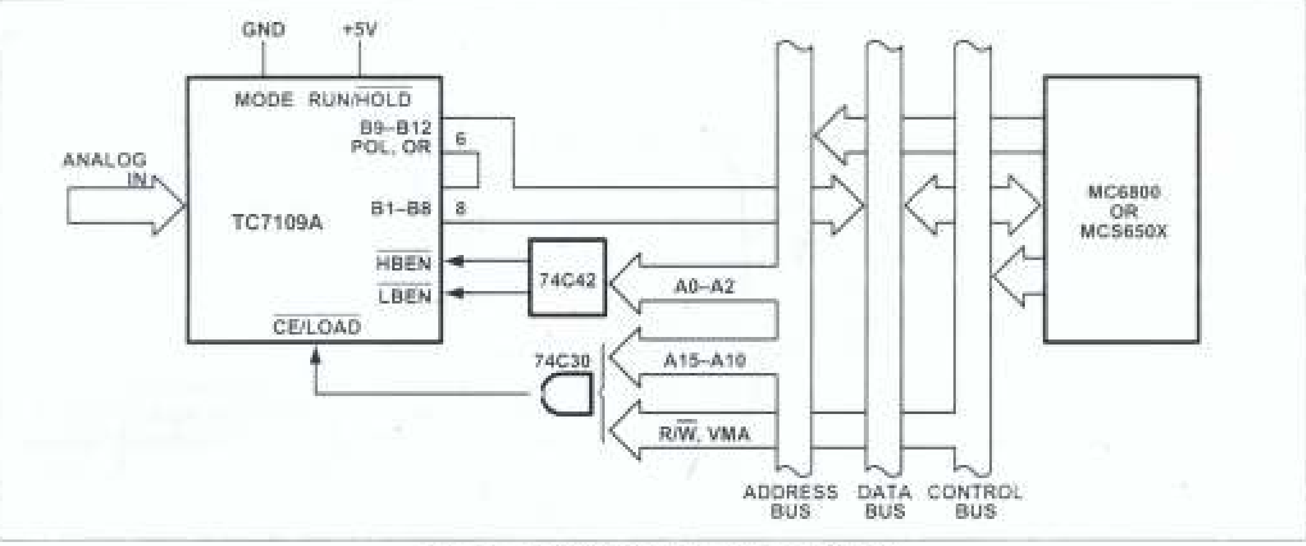


Figure 18. TC7109A Direct Interface to MC6800 Bus

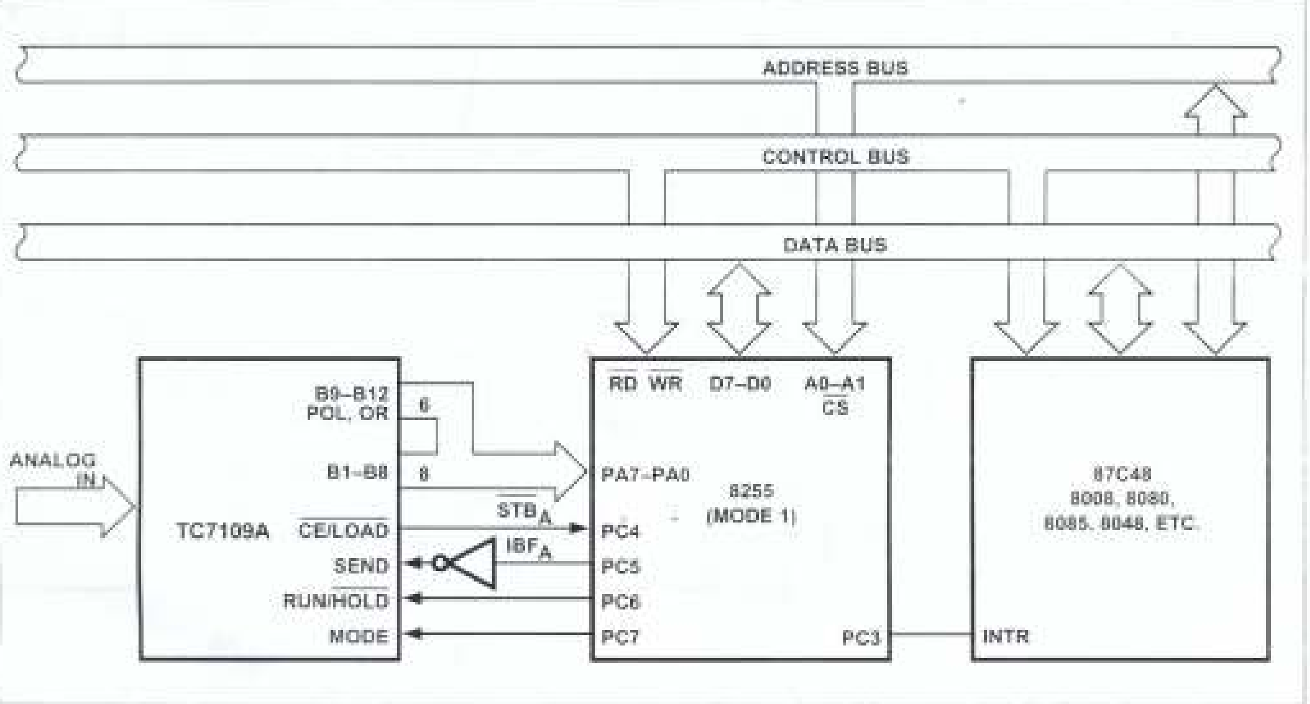


Figure 19. TC7109A Handshake Interface to MCS-48, -80, -85 Microcomputers

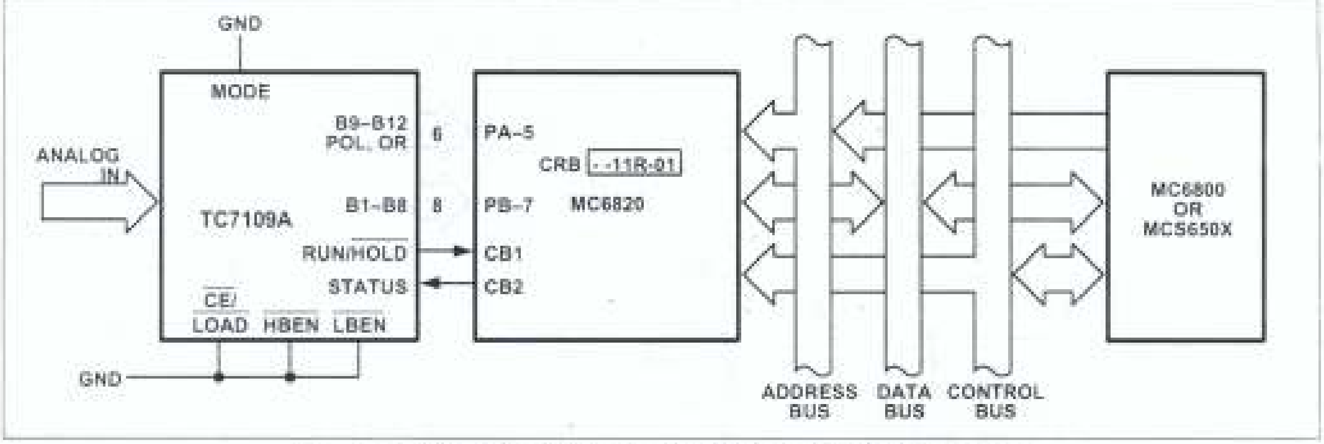
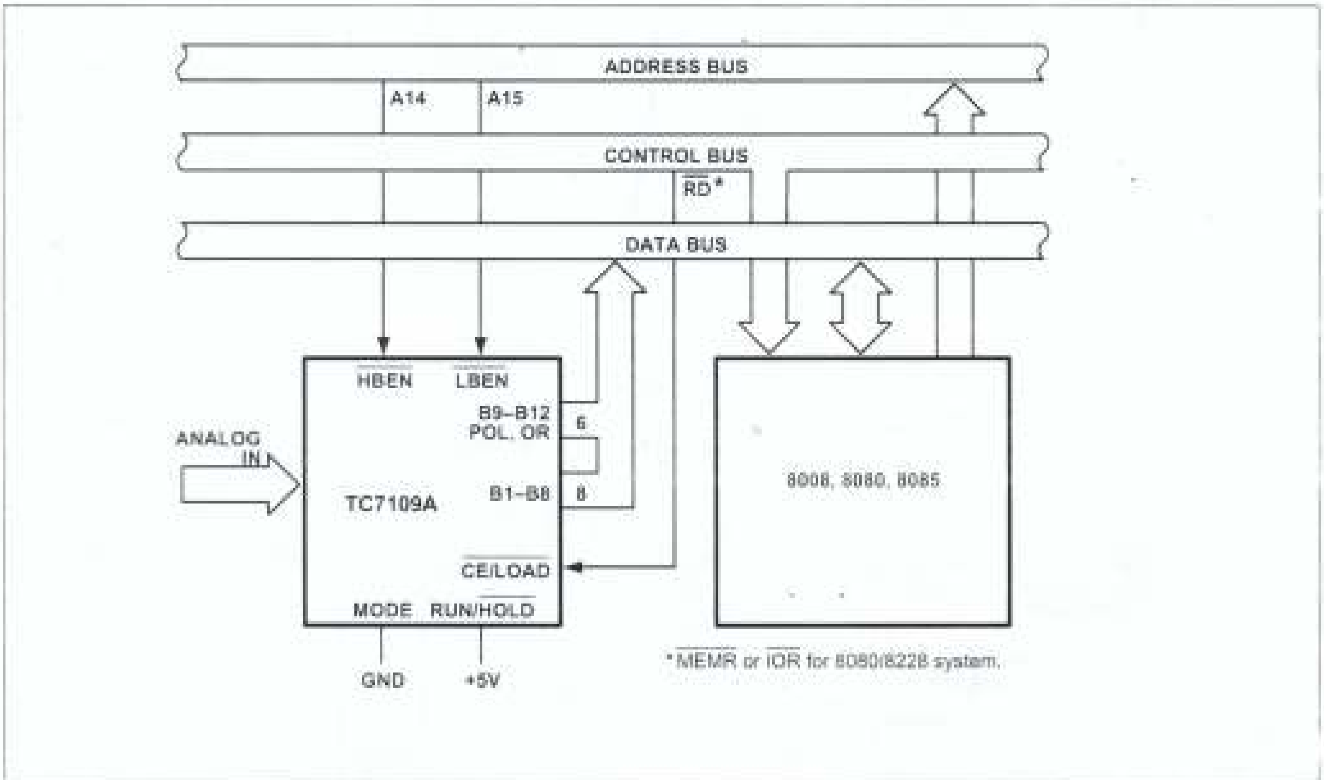


Figure 16. Full-Time Parallel Interface to MC6800 or MCS650X Microprocessor



*$\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ for 8080/8228 system.

Figure 17. TC7109A Direct Interface to 8080/8085

Handshake Mode

The handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of CE/LOAD. A handshake interface to Intel microprocessors using an 8255 PPI is shown in Figure 19. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TC7109A, and using the CE/LOAD to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is LOW and the TC7109A is in handshake mode, the next word will be strobed into the port. The strobe will cause IBF to go HIGH (SEND goes LOW), which will keep the enabled byte outputs active. The PPI will generate an interrupt which, when executed, will result in the data being read. The IBF will be reset LOW when the byte is read, causing the TC7109A to sequence into the next byte. The MODE input to the TC7109A is connected to the control line on the PPI.

The data from every conversion will be sequenced in two bytes in the system, if this output is left HIGH, or tied HIGH separately. (The data access must take less time than a conversion.) The output sequence can be obtained on demand if this output is made to go from LOW to HIGH and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/HOLD input to the TC7109A by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255. The 8155 may be used in a similar manner. The MCS650X microprocessors are shown in Figure 20 with MODE and RUN/HOLD tied HIGH to save port outputs.

The handshake mode is particularly useful for directly interfacing to industry-standard UARTs (such as Western Digital TR1602), providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure 1. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go HIGH. The MODE input to the TC7109A goes HIGH, triggering the TC7109A into handshake mode. The high-order byte is output to the UART and when the UART has transferred the data to the Transmitter register, TBRE (SEND) goes HIGH again, LBEN will go HIGH, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the TC7109A to the UART.

An extension of the typical connection to several TC7109A's with one UART is shown in Figure 21. In this circuit, the word received by the UART (available at the RBR outputs when DR is HIGH) is used to select which converter will handshake with the UART. Up to eight TC7109A's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.

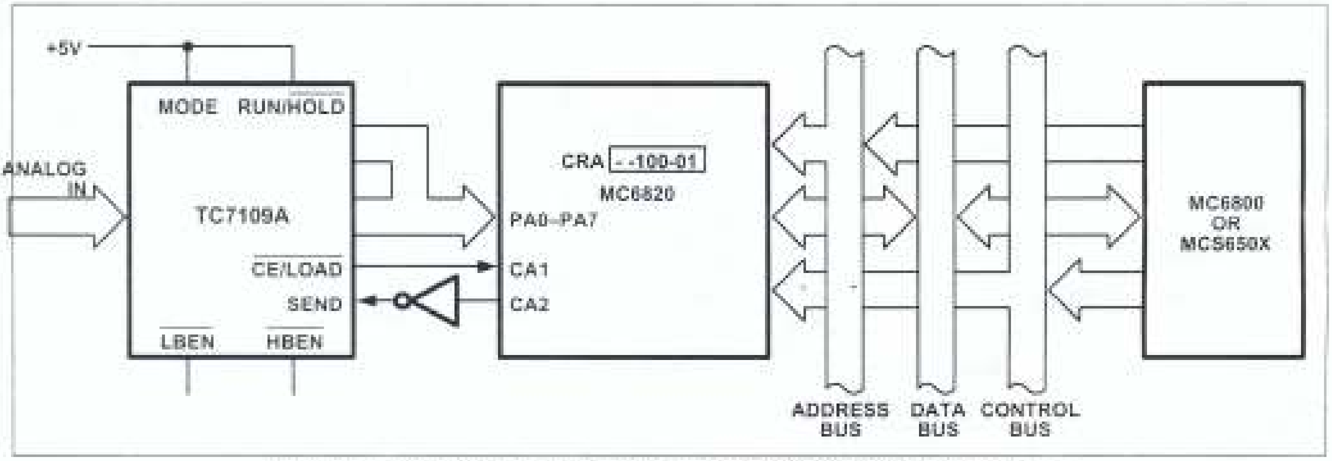


Figure 20. TC7109A Handshake Interface to MCS-6800, MCS650X Microprocessors

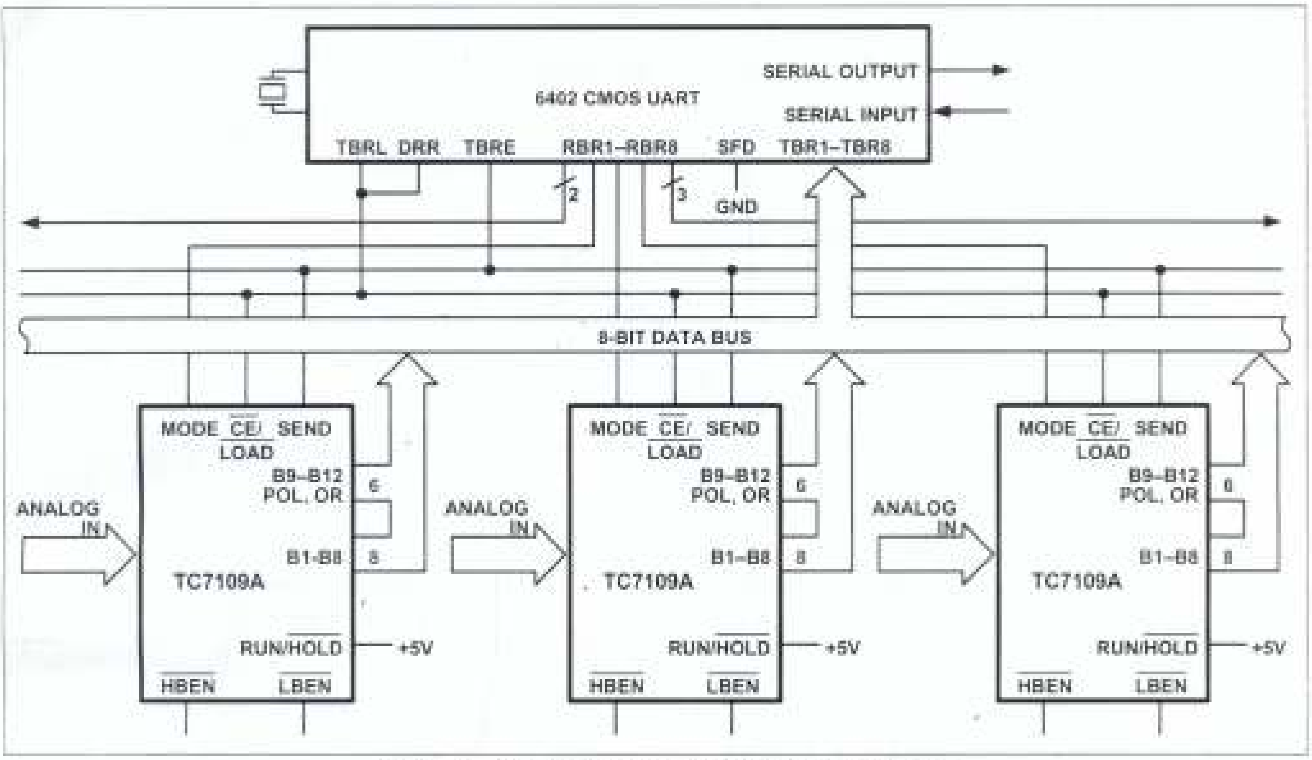


Figure 21. Handshake Interface for Multiplexed Converters

Integrating Converter Features

The output of integrating ADCs represents the integral, or average, of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter averages the effects of noise. A second important characteristic is that time is used to quantize the answer, resulting in extremely small nonlinearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise (Figure 22).

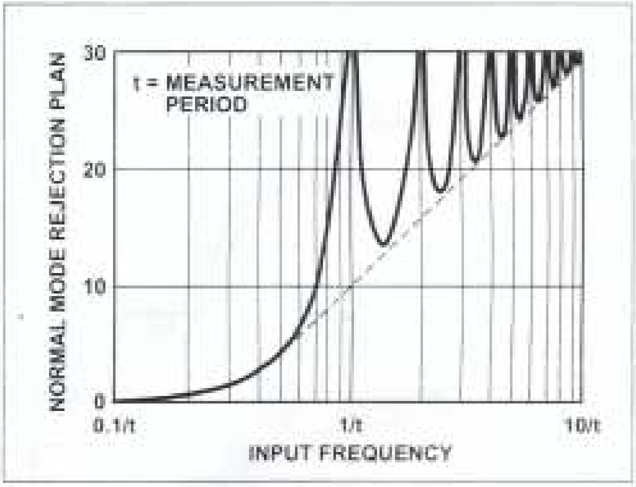
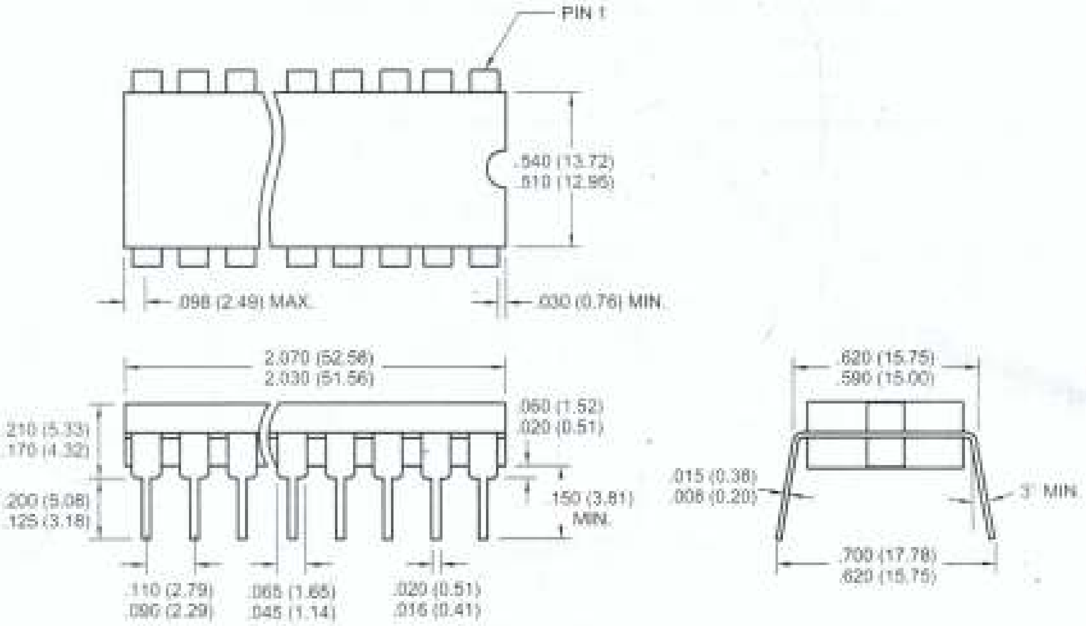


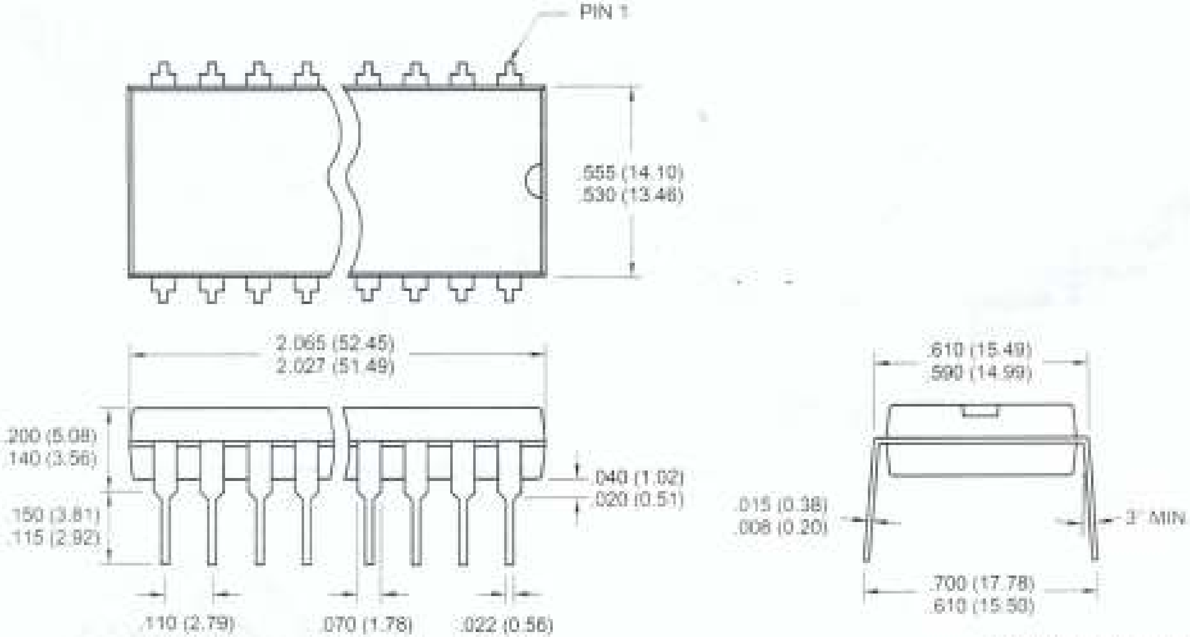
Figure 22. Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency

PACKAGE DIMENSIONS

40-Pin CDIP (Wide)



40-Pin Plastic DIP



Dimensions: inches (mm)