DESIGN, CONSTRUCTION AND EVALUATION OF A DIGITAL CONTROLLER FOR A WASHING MACHINE

BY

OLADEJO, ISMAHEEL OYEYEMI (EEE/97/9905)
(B.Eng.)

A THESIS SUBMITTED TO

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CERTIFICATION

This is to certify that Oladejo, Ismaheel Oyeyemi (EEE/97/9905) carried out this work under my supervision in the department of Electrical/Electronics Engineering of the Federal University of Technology, Akure.

EGNR. (PROF.) S.O. FALAKI
SUPERVISOR

DATE: 26/10/03

DR. V. S. A. ADELOYE
HEAD OF DEPARTMENT

DATE: 6-10-2003

.....
EXTERNAL EXAMINER

DATE:.....

DEDICATION

This thesis is deservedly dedicated to my late father Mr. Sanni Oladejo (may his gentle soul rest in peace) Amen.

ACKNOWLEDGEMENT

My greatest gratitude goes to the Almighty Allah for sustaining my life throughout the duration of my programme in this institution.

I am particularly indebted to my able, hardworking and articulate supervisor Engr. (Prof.) S.O. FALAKI and co-supervisor Engr. J.O. Oni whose encouragement, criticism and patience in seeing through the design and construction of the project were instrumental to the success of the project.

I acknowledge the invaluable assistance rendered by Tunde Olajide (Coach) whom God has used in assisting me both morally and academically.

I should like to register my deep appreciation to Mr. Odeleye Seye for assisting me in this project.

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To crown it all, I thank my wife Mrs. Oladejo Omolara for her support both morally and financially for the successful completion of the programme.

ABSTRACT

This project is aimed at improving the Control System of a washing machine. A new Control system was designed and Constructed. Unlike some conventional models in the market which, make use of electromechanical control, this design is purely electronics and it displays the mode and type of fabrics to be washed, which are added features.

Additional facility was also incorporated into the system which enable a particular process to be repeated and this is done by the use of presettable up/down counter.

As opposed to the conventional model, different type of fabrics have different decoding time cycle, that is to say that average washing period varies from one fabric to the other. Also the device is cheaper, simpler and convenient as opposed to the conventional mode.

The system also offers greater flexibility since it can be adapted to control some other equipment like automatic electric mixer etc.

In this project, the principle of operation, the design and performance evaluation were considered in details.

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LIST OF SYMBOLS

D.C – Direct current

A.C – Alternating Current

I.C – Integrated Circuit

Hz – Hertz

KHz – Kilo – Hertz

MHz – Mega Hertz

GHz – Giga Hertz

R.M.S – Root Mean Square

TTL – Transistor Transistor logic

LED – Light Emitting Diode

LSB – least significant Bit

MSB – Most Significant Bit

FF – Flip Flop

CK – Clock

No – Normally Open

Nc – Normally Closed

PLA – Programmable logic Array

BCD – Binary Coded Decimal

AMF – Astable Multivibrator

VCO – Voltage Control Oscillator

Tr – Transistor

PCB – Printed Circuit Board

CHAPTER ONE

PROJECT BACKGROUND

A digital controller that was designed and constructed is device which is used to control washing machine for washing cloth of different fabrics.

A major part of the system consists of electrical and electromechanical components such as motors, valves and heaters. These could be controlled by electromechanical or electronic system which in turn is operated by signals from an electronic controller. Other signals will be fed to the controller from manually selected inputs. The electronic controller must have a MEMORY to know which state it is in which state it must change to and when it is to change (as a result of sensor signal or a timer). As the controller changes state, it must generate and direct control signals to the relays operating motors and heaters.

The washing machine is operated in the following manner. After loading the clothes into the washing chamber of the machine, the soap, or detergent, bleach and water are introduced in the proper amount. The washing and wringing cycle time is then set on a timer and the washer is switched on. When the cycle is completed, the machine shut itself off.

The device is calibrated by estimating any combination of the following input quantities (1) Amount of detergent (2) Amount of bleach (3) Amount of water (4) Temperature of water (5) Cycle time.

Some of these input quantities like temperature of water and cycle time are predetermine during the design of the project, the remaining quantities are estimated by the users depending upon the factors such as degree of hardness of water, type of detergent and type or strength of bleach. Once this calibration has been determined for the specific type of

wash, it does not normally have to be predetermined during the life time of the machine. If the machine breaks down and replacement part are installed recalibration is probably necessary.

1.1 PROJECT MOTIVATION

In recent times and even these days, investigation reveals that most homes (most especially in Nigeria) have been using hands, brushes e. t. c. in washing materials of their cloth. This may probably due to the fact that they are ignorant about the existence of the washing machine. Moreover, the washing machines that are used in most homes are very expensive i.e. the cost of purchasing an already made imported washer is enormous. Not only that most of the components used are not readily available in our local market while importing them requires high cost.

It is therefore the purpose of this project to design electronic controller for this device that is purely electronic-controlled, cheaper, simpler and also offer the advantages of self starting without any need for auxiliary equipment.

It is also portable, very efficient and easy to maintain. The manufacturing cost is economical and is within the reach of the average Nigerian. It is also reliable with readily available component such as relays, 555 timer, high speed motor, electric heater etc.

1.2 OBJECTIVE AND SCOPE OF THE PROJECT

The objective of this project is to design and construct a sizeable and cheap electrically operated device for washing clothes of different fabrics. This could be achieved by putting machine in a series of (menu-driven) logically controlled state e.g. inlet valve

OPEN, heater OFF, motor OFF; inlet valve CLOSED, heater ON, motor ON; inlet valve CLOSED, heater OFF, motor OFF, outlet valve OPEN; etc. The duration of each state will be determined by a pre-selected timer.

The sequence of operation of the device is thus:

1. Fill the washing chamber with water and detergent.
2. Raise and maintain the temperature of water at a preset level
3. Agitate the water for a specified time
4. Remove hot soiled water
5. Rotate the chamber at high speed for a preset time
6. Finally to prevent opening of the chamber until the device is brought to a stand still with all the water expelled.

In summary, the specific objectives of the research are:

(a) To design and construct analog to digital conversion process used in controlling washing machine.

(b) To design and construct stabilized power supply unit for the system.

(c) To determine the particular electric motor to be used in order to produce rotational motion as opposed to pulsating motion when a single phase is applied.

(d) To design and construct for an interface circuit

(e) To evaluate the performance of the device.

1.3 RESEARCH METHODOLOGY

In pursuance of the said objectives, the evaluation of control process and the determination of timing to be used in washing different fabrics was first carried out and then followed by the design of various units such as power supply unit, programmable logic control unit, interface unit and various process indicators. The assembly of the various components and construction of the device and the housing were carried out in line with the stated objectives.

1.4 EXPECTED CONTRIBUTION TO KNOWLEDGE

The project will

- Establish the different decoding time cycles and hence duty cycles for various fabrics by using clock generator, modulo 60 counter and frequency divider.
- Produce relatively low cost and portable machine.

1.5 OUTLINE OF THE PROJECT

In chapter two, a literature review of controller technique is presented. Different types of controller, analog controller display and general digital process controller are discussed chapter three deals, with component analysis and design of power supply unit.

Chapter four deals with the analysis and design of the functional component making up the timing circuit.

Chapter five took a look at analysis and design of counter. In this case divided by 60 counter, variable frequency divider, multiplexer and demultiplexer are fully discussed. In chapter six, analog to digital conversion process of washing machine is presented. The analysis, design and operation of logic control microprocessor, programmable logic array, interface circuit and presettable up/down counter are well presented.

In chapter seven design and constructional consideration, performance evaluation and costing of the device are discussed. Chapter eight contains conclusion and recommendation.

CHAPTER TWO

LITERATURE REVIEW

INTRODUCTION

General-purpose process controller originated in pneumatic form about forty five years ago. Subsequently, these were superseded by electronic versions, to a large extent, using firstly discrete, component and then integrated circuit analog technology. Because of cost and reliability, recent development has involved synthesizing the controllers with digital hardware with control law hardwired (Chesmon, 1993). The progressively increasing degree of complexity and sophistication has presented potential problem in terms of maintenance, fault location, and repair, and these become significant factors when selecting a controller.

2.1 TYPE OF CONTROL ACTION

Process controller can be subdivided into feedback, cascade, feed forward and ration controllers depending upon the type of action which each is required to provide.

The application of a feedback controller which was used in the project is shown in fig. 2.1 such controller makes provision for setting the desired value (called the "set point"), accepting the measured value from feedback transducer, determining the difference (called "the error" or "deviation") and thereby generating an output signal which is related to the deviation by a preset algorithm. This algorithm usually includes time-dependent terms thereby providing dynamic compensation of the control loop.

2.2 *ANALOG CONTROLLER DISPLAY*

Analog display is incorporated to the faceplate of a controller. This system employs solid state "thermometer" type of scale using sets of parallel light - emitting diode. In some cases a system may prefer to use miniature gas-discharge indicators each taking a form of a very short bar to represent a specific signal level.

The variables usually displayed are set point, deviation, process variable and controller output. Controllers often include means to indicate when deviation exceeds manually pre-set upper and lower limits, and, in addition, simultaneous output signal may be generated in order to activate remote alarm alternatively, the alarm indicator may be monitoring either the process variable or the controller output.

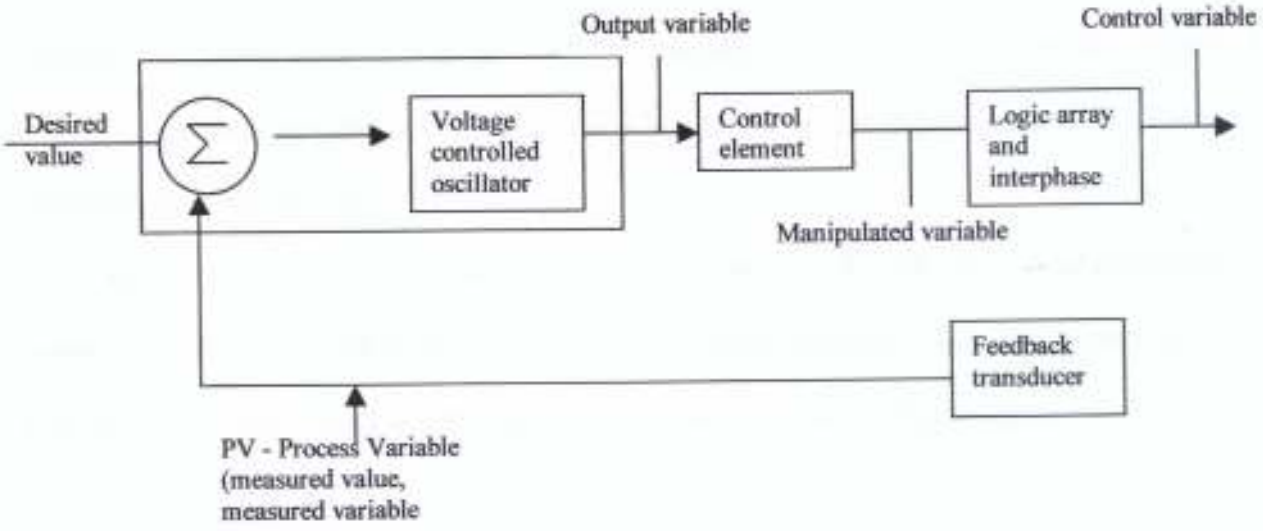


Fig. 2.1: Block Diagram of a Feedback Controller

2.3 *DIGITAL PROCESS CONTROLLER*

The availability of digital hardware has introduced improved reliability and flexibility to the production of a process controller.

Where the number of control loops for a particular plant is small, it is becoming common practice to install, in the place of analogue controller an equivalent digital controller (Nagrath and Copal 1992). With this approach, the digital controller would be designed to synthesis its analog counter part and would resemble it physically, in terms of external connection, such controllers are microprocessor based, with a separate micro-processor being dedicated to each controller.

Since in the project, the number of control loop exceeds eight the use of electronic system come to play in which the microprocessor is shared between a number of controllers. This approach offers much greater flexibility. Moreover, the configuration can be revised easily at a later stage should this be desired.

The distributed control system is undertaken in stages: taken in chronological sequence, these would involved controller configuration and intercommunication, followed by specification of ranges etc. All such data would be entered manually, in the form of an alphanumerical code, and stored in semi-conductor memory. Typically, communication between controllers and plant would be by means of analog signal transmission; communication between controllers and situated within the same logical grouping would be by means of parallel digital data transmission (Chesman, 1993).

Introduction of digital controllers involved a number of types of decision which are not relevant to the selection of their analog counter parts.

2.4 HEAT CONTROL

The function of a temperature controller is to switch on and off a source of heating or cooling. The design is undertaken most readily with relays and/or contactors in the case of electric heaters. An alternative is to use Triac or SCR networks, with the thyristor being gated on and off by a suitable drive network. Reliability and maintainability will be high with power semi-conductors provided that they are protected against excessive transients; the fact that a heater is almost purely resistive assists in this respect.

CHAPTER THREE

STABILISED POWER SUPPLY UNIT

3.1 CIRCUIT DESCRIPTION

Fig 3.1 and the circuit diagram of fig 3.2 will aid this description. It consists of four distinct units viz:

(a) Transformation unit

(b) Rectification unit

(c) Filtration unit and

(d) Regulation / Stabilization unit

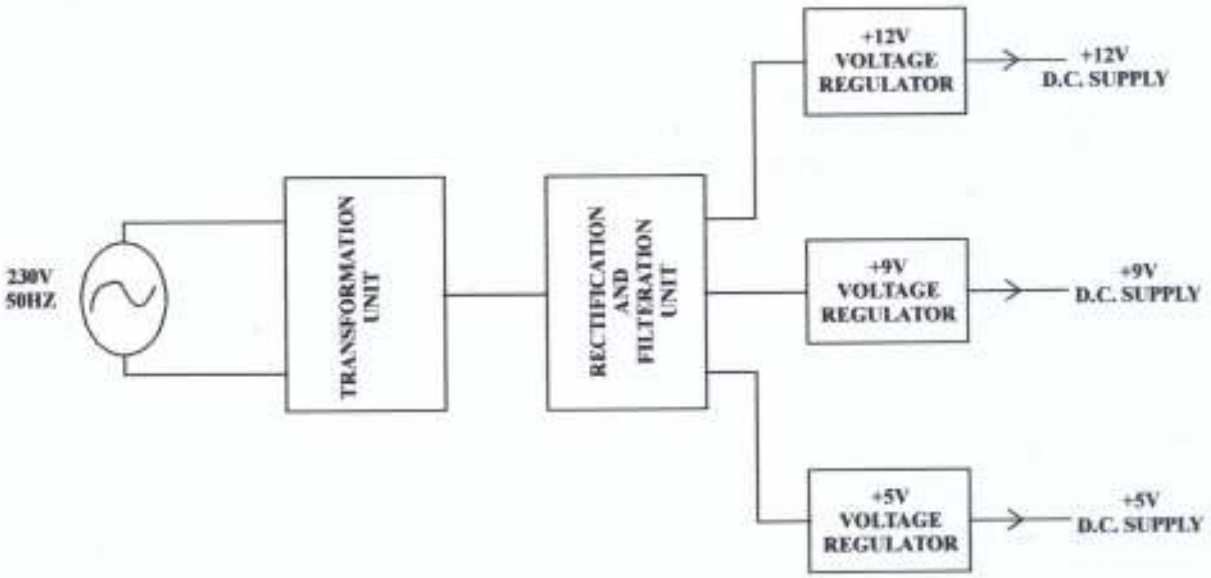


Fig 3.1: Block Diagram of Stabilized Power Supply System

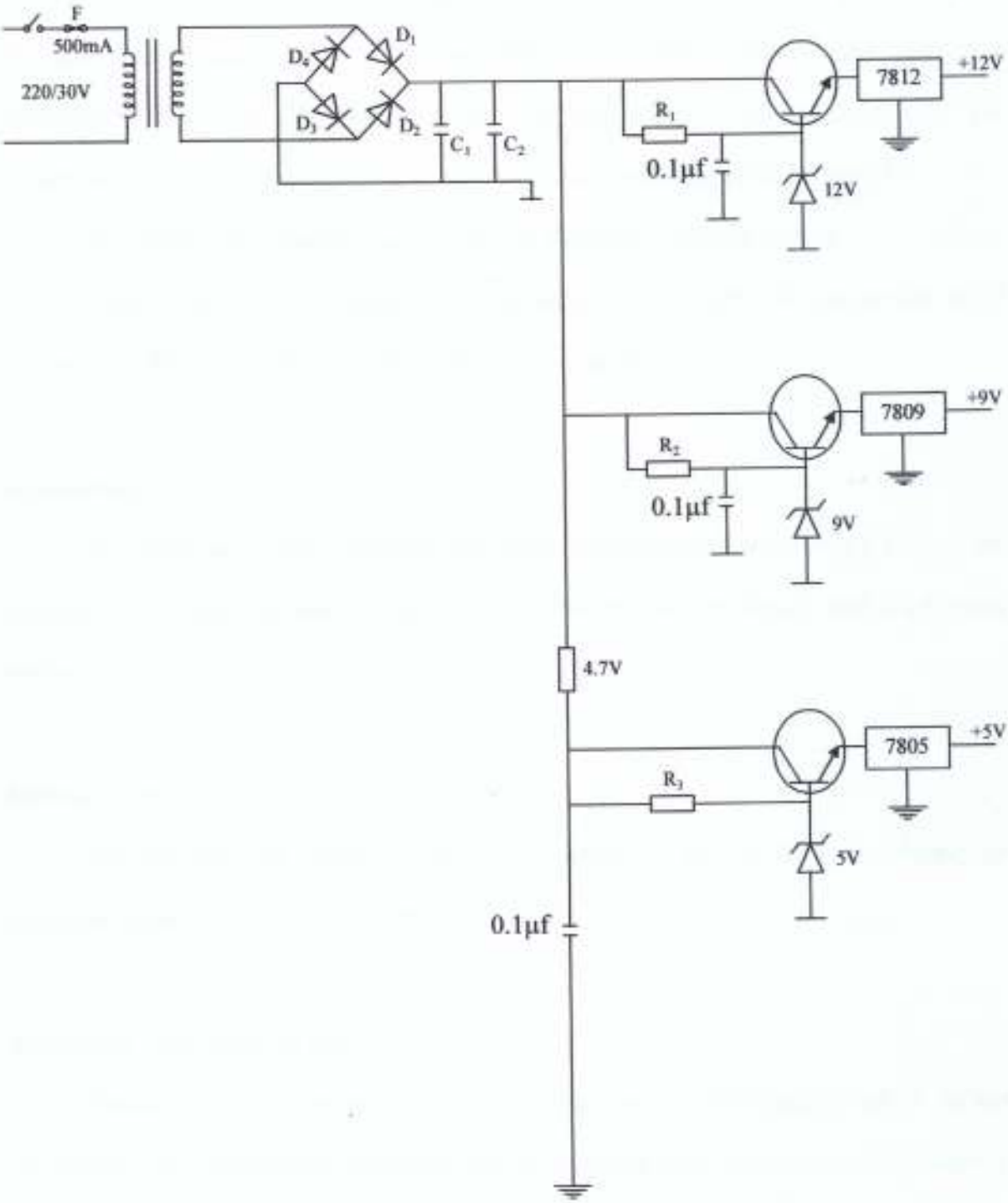


Fig. 3.2: Power Supply Unit

Transformation Unit

The transformer unit consists mainly of a step down transformer T_1 (i.e. 230V a.c / 30V a.c). The secondary terminal of the transformer is connected to the Bridge rectifier. The secondary voltage is usually specified by full load, and will rise with decreasing load. The variations of output voltage with load is specified by the regulation which is defined as:

Regulation = (Off load Voltage – Full load Voltage) / Off load Voltage

Typical values for the regulation are between 10% and 20%. The protective device consists of a 500mA fuse for slow blow 240volts a.c supply.

Rectification Unit

The rectification unit comprises of a bridge rectifier which converts a.c voltage into pulsating d.c voltage. The circuit employs four diodes but the transformer used is not center tapped and has a maximum voltage of V_m.

Filtration Unit

The filtration unit which consists of Capacitors C_1 and C_2 helps in reducing the unwanted ripple content of the rectified a.c.

Regulation / Stabilization Unit

Regulation / Stabilization unit is designed together on silicon chip to reduce the size and weight. The LM series of monolithic voltage regulator were used instead of the shunt or series voltage regulators that utilize discrete components. The voltage regulators ensure that

the output voltage does not drift when there is increase or decrease in output load current or when there is increase in input voltage.

3.2 PRINCIPLE OF OPERATION OF THE POWER SUPPLY

The mains of the power supply (i.e. 220V a.c / 50Hz) is taken from a.c source through a 500mA fuse to a step down transformer T_1 (i.e 220V a.c / 30V a.c). The output of the transformer is fed to a bridge rectifier which rectifies the a.c to d.c.

At the positive half cycle of the input, the bridge rectifier, supplies a 27V d.c peak voltage, which is fed through a filtering capacitor C_1 and C_2 with value 600μF, 50V to the voltage regulator LM1 (7812) thus producing constant +12volts d.c output as shown in fig.3.2 Likewise, part of the output of the bridge rectifier is fed via a filtering unit to another voltage regulator LM2 (7809) and LM3 (7805) to produce a constant of +9volts d.c and +5volts d.c supply respectively as shown in the circuit of fig. 3.2.

3.3 DESIGN METHOD AND MATERIALS

In this project, the design of stabilized power supply is made up of monolithic regulator (LM-Series). The design procedure involved the mathematical analysis of the practical power supply.

3.3.1 THE TRANSFORMATION UNIT

A 230 / 30V a.c, 2 ampere transformer was used in the design of power supply.

3.3.2 PROTECTION

As a protective device, a slow blow 500mA fuse was used at the input of the 230volts transformer. (see fig. 3.2)

3.3.3 RECTIFICATION UNIT

A bridge rectifier diodes D used in this project was chosen with the following ratings to withstand surge from the input supply.

Peak Inverse Voltage, PIV = 50V

Current Rating = 2A

Voltage drop / diode = 1.4volts

(floyd 1999)

The bridge rectifier employed provided the required +12, +9 and +5 volts supplies.

3.3.4 SHUNT INPUT CAPACITOR FILTER

To determine the filter capacitor. The a.c voltage from Transformer is assumed to be a perfect sinewave, hence for a full-wave rectifier the curve in fig 3.3 was used to specify the filter capacitor. (OLADEJO 1989).

The rectifier used was a bridge rectifier of forward drop of (0.7x2) V = 1.4V

The filter capacitor used is such that it can give a maximum ripple of 7% on the positive supply since the transformer voltage is 30v, the peak voltage on the filter capacitor is given by

$(30\sqrt{2} - 1.4 = 41.02V)$

i.e.

V bridge = V peak – V diode

Percentage ripple is given by

% Ripple = ΔV_C/Vmax X 100 ..... 3.1

where ΔV_C is the peak to peak ripple voltage

:- for 7% ripple

Ripple voltage = 7/100 x 41.02/1

= 2.87V 3.2

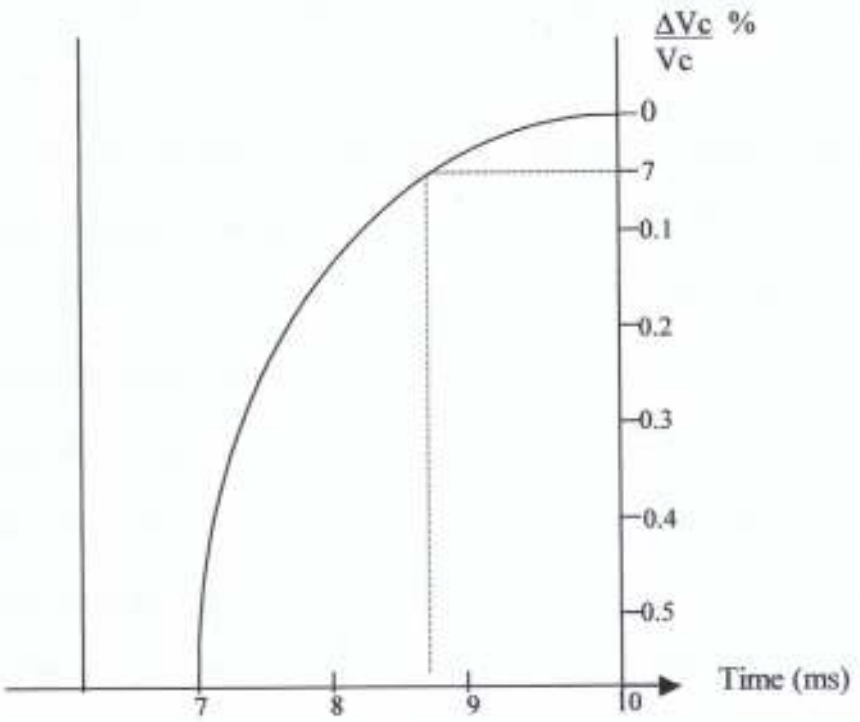
The value of capacitance is given by

$C = I_0 \times \Delta t/\Delta Vc$

where I_0 is the maximum load current and Δt is the time taken to reach 7% ripple from the curve in fig 3.3

Δt =8.7ms and I_0 = 2A

C = 607μf



$$\% \text{ ripple} = \frac{\Delta Vc}{Vmax} \times 100\%$$

Fig. 3.3: Sinewave for Capacitor Selection

From the standard catalogue, 6000uF of 50V electrolytic capacitor was selected.

3.3.5 VOLTAGE REGULATORS

The required output voltages are +12V, +9V and +5Volts all of which should have maximum current rating of 1000mA.

The following specifications are typical for most of the regulators used

Output Voltage Tolerance	1 – 2%
Drop out Voltage	0.05 – 2volts
Maximum Input Voltage	35volts
Ripple Rejection	0.01 – 0.1%
Spike Rejection	0.01 – 0.3%
Load Regulation	0.1 – 0.5% Full load charge
D.C Input Injection	0.2%
Temperature	0.5% over full temperature range

Features

- Internal thermal overload protection
- No external components required.
- Output transistor safe area protection.
- Internal shunt circuit current limit.

Voltage Range

7805 – 5V

7812 – 12V

7809 – 9V

From fig 3.2 the value of resistor R_1 for 12V emitter follower stabilizer can be calculated thus:

The condition imposed by the transistor for itself is

$$I_C = hfe\ I_B \text{ ----------3.4}$$

Since the transistor used is BD131 with the following parameters

Ic(max) = 3A, hfe = 400 and the zener diode has Vz = 12volts and Iz = 7mA.

By equating the sum of voltage drop across R_1 and Zener diode to the collector supply voltage, we obtain

$$V_{CC} = V_{R1} + V_Z \text{ ----------3.5}$$

With V_{CC} = 27volts

V_{R1} = 15volts

By substituting for hfe and I_C in equation 3.4, we have

I_B = 6mA

Also $I_{R1} = I_B + I_Z$ ----------3.6

= 13mA

Therefore,

$$R_1 = V_{R1} / I_{R1} = 1154 \text{ ----------3.7}$$

R_1 was selected to be 1.5KΩ

Similarly, R_2 in fig 3.2 can also be calculated thus:

With the same parameter as above but with V_Z = 9V and I_Z = 5mA.

By substituting in equations 3.4, 3.5, 3.6 and 3.7, we shall have

I_B = 7.5mA, V_{R2} = 18V, I_{R2} = 12.5mA and R_2 = 1.4kΩ

Therefore, R_2 was selected to be 1.5kn.

Also, R_3 in fig 3.2 can also be calculated thus:

With the same parameter as above, but $V_Z = 5_V$ and $I_Z = 5mA$

By substituting in equations 3.4, 3.5, 3.6 and 3.7, we have:

$$I_B = 7.5mA,\ V_{R3} = 22V,\ I_{R3} = 12.5mA \text{ and } R_3 = 1760\Omega$$

R_3 was selected to be $2k\Omega$.

CHAPTER FOUR

OPERATIONAL ANALYSIS AND DESIGN OF TIMING CIRCUIT

This chapter deals with the analysis and design of the functional components making up the timer. It is this timer that generates the clock input necessary to operate the counter.

4.1 INTEGRATED CIRCUIT TIMER

The most widely used integrated circuit (IC) timer is the IC555 which was introduced by signetic corporation. This IC has 8 pins. Details regarding connections to be made to pins are as follows:

Pin 1: This is the ground pin and should be connected to the negative side of the supply voltage

Pin 2: This is to trigger input

Pin 3: This is the output pin and is capable of sinking or sourcing a load requiring up to 200mA and can drive TTL circuits.

Pin 4: This is the reset pin and is used to reset the flip-flop that controls the state of output pin 3.

Pin 5: This is the control voltage input. The voltage applied to this pin allows device timing variations independent of the external timing network.

Pin 6: This is the threshold input. It resets the flip-flop.

Pin 7: This is the discharge pin. It is connected to the collector of an NPN transistor while the emitter is grounded.

Pin 8: This is power supply pin and is connected to the positive side of the supply.

The IC555 timer consists basically of two comparators, a flip-flop, a discharged transistor and a resistive voltage divider as shown in fig 4.1.

A flip-flop is a digital device. It is a two state device whose output can be at either a high voltage level (set) or a low voltage level (reset). The state of the output can be changed with proper input signals.

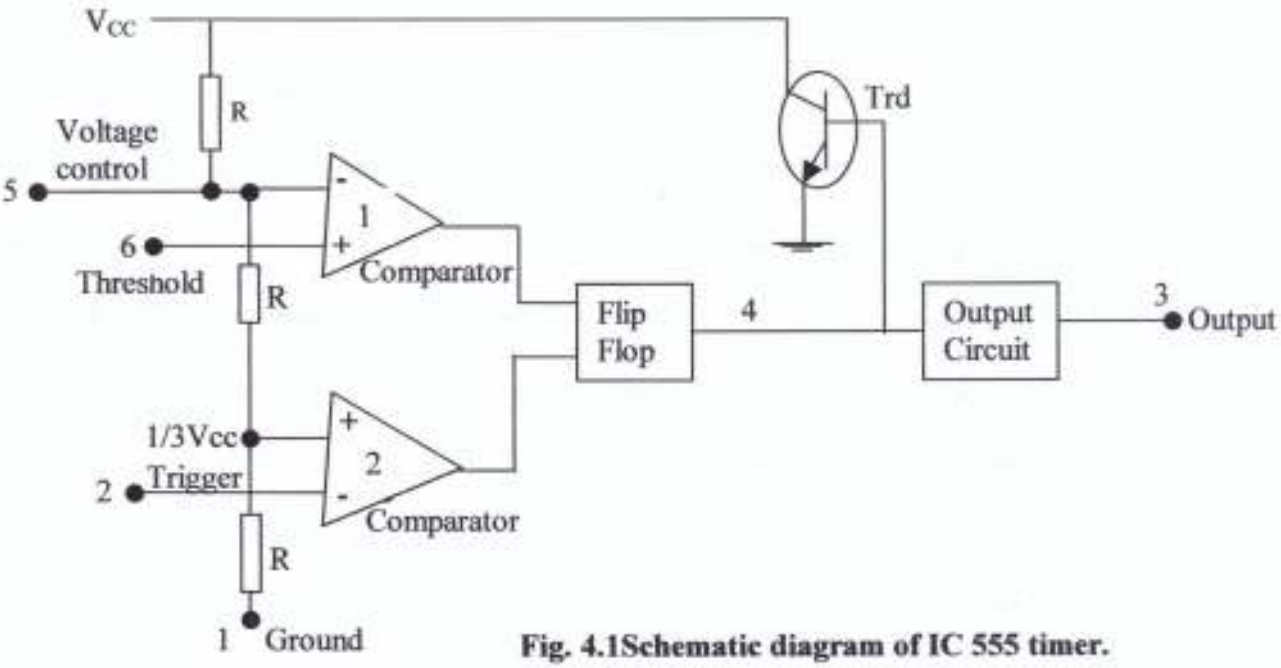


Fig. 4.1Schematic diagram of IC 555 timer.

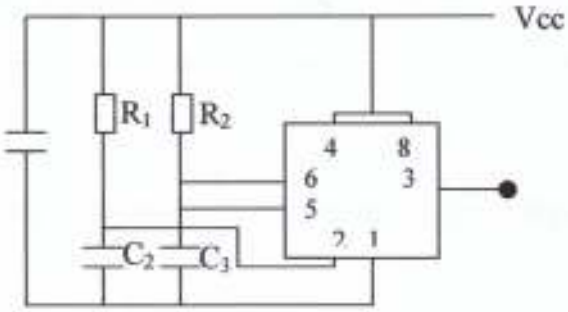


Fig. 4.2: IC 555 Configured for Monostable - Operation

The resistive voltage divider is used to set the voltage comparator level. All three resistors are of equal values, therefore the upper comparator has a reference of 2/3 V_{CC} and the lower comparator has a reference of 1/3 V_{CC}.

The comparators outputs control the state of the flip-flop. When the trigger voltage goes below 1/3 V_{CC}, the flip-flop sets and the output jumps to its high state/level. The threshold input is normally connected to an external R_C timing network. When the external capacitor voltage exceeds 2/3 V_{CC}, the upper comparator 1 reset the flip-flop which in turn switches the output low. The discharged transistor Trd is turned ON and provides a path for rapid discharge of the external timing capacitor.

4.1.1 IC555 AS A MONOSTABLE MULTIVIBRATOR (ONE SHOT)

By connecting an external resistor and capacitor to the IC555 timer as shown in fig 4.2, monostable (one-shot) operation is achieved.

One shot (monostable) operation is when a short duration negative pulse is applied to the trigger input, a single positive pulse is produced on the output. The duration of this output pulse is set by the value of the external resistor (R) and capacitor C. The operation is as follows:-

The flip-flop is initially set causing the device output to be high when the trigger input goes below 1/3V_{CC}.

4.1.2 IC 555 AS AN ASTABLE OPERATION

An IC555 timer connected to operate in the astable mode as a free-running non-sinusoidal oscillator is shown in fig 4.3.

In astable multivibrator operation, the threshold input is connected to the trigger input initially. When the d.c power is turned ON, the capacitor is discharge and holds the trigger voltage at less than 1/3 V_{CC}. This level triggers the lower comparator, causing the output to switch high and Trd to turn OFF. Now Cext begins charging through R_1 and R_2. When the capacitor voltage reaches 2/3 V_{CC}, the output switches low and Trd turns ON. Cext now discharges through R_2 and Trd.

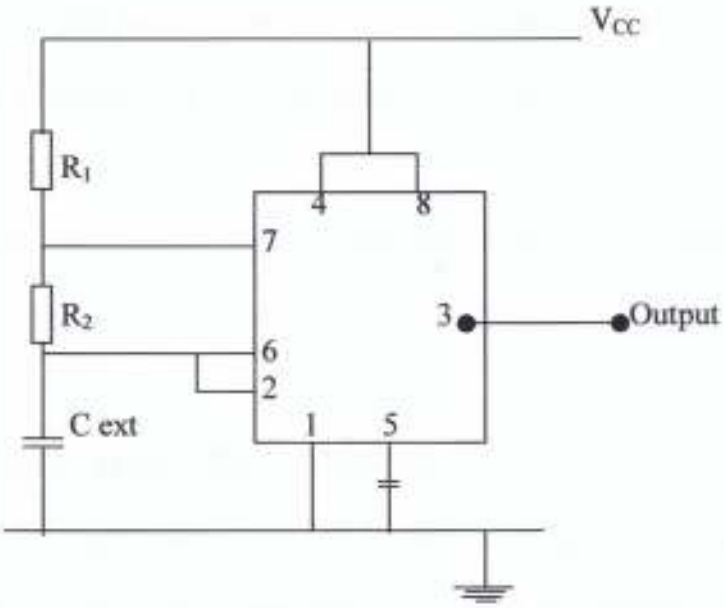


Fig 4.3:- IC555 Configured For Astable Operation

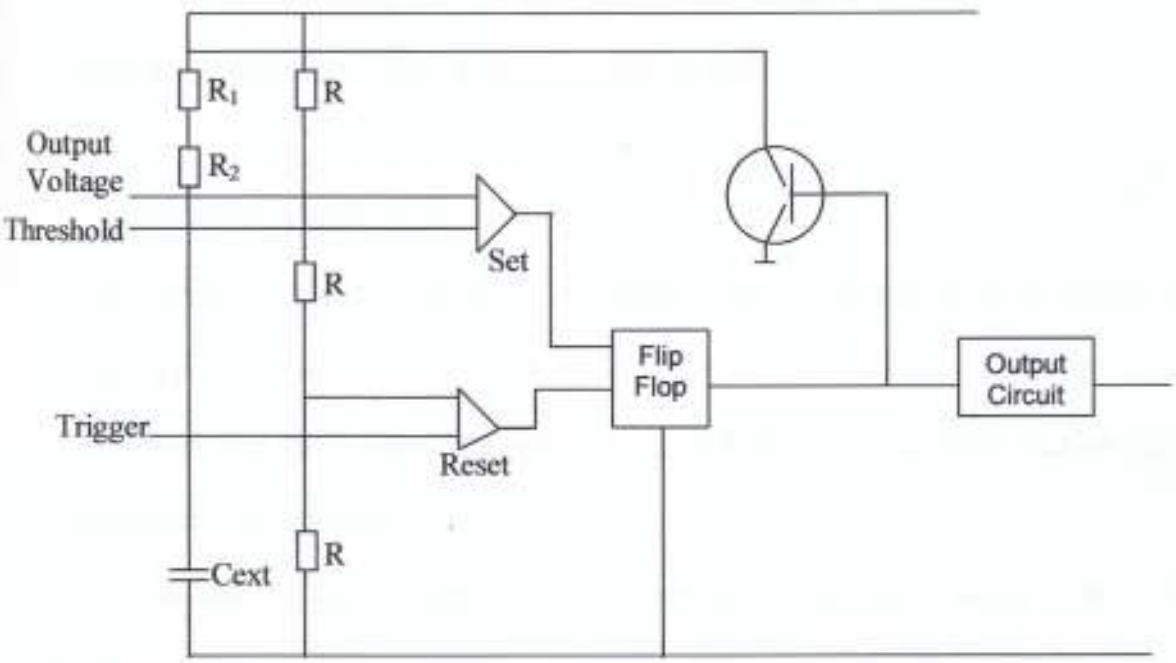


Fig. 4.4:- Schematic Diagram of IC555 as Astable Multivibrator

When the capacitor voltage decreases to 1/3 V_{CC}, the lower comparator again triggers, causing the output to switch back high and turn off Trd. The cycle now repeats itself, and the device oscillates.

Note that the voltage control input is decoupled to the ground, since it is used as AMF and not voltage control oscillator (VCO).

4.2 CLOCK GENERATOR CIRCUIT DESIGN

In designing a clock generator circuit (which was used to generate a clock to the counter in the project) an astable multivibrator otherwise called free-running multivibrators were used. The 555 timer I.C used is a TTL compartible device that can operate in several different modes.

Fig 4.4 shows how external component can be connected to a 555 timer so that it operates as a free-running multivibrator. However to get very close to 50% duty cycle $R_2 >> R_1$ (while keeping R_1 greater than 500Ω), so that $t_1 \approx t_2$ (Floyd 1999).

DESIGN CALCULATION

To design a clock generator circuit using a 555 timer connected in astable mode, frequency of 8Hz was choosen.

In this design, Pin 5 was connected to the ground through a capacitor of about 0.01μf to suppress the effect of noise

The time T_1 that the output is high is how long it takes Cext to charge from 1/3 V_{CC} to 2/3 V_{CC} i.e.

$$T_1 = 0.693 (R_1 + R_2) Cext \quad (4.1)$$

Since Cext charges through R_1 and R_2. The time T_2 that the output is low is how it takes Cext to discharge from 2/3 V_{CC} to 1/3 V_{CC}.

$T_2 = 0.693\ R_2\ Cext$ ..... (4.2)

Since C ext discharges only through R_2. The period of the input waveform is the sum of T_1 and T_2.

i.e. $T = 0.693\ (R_1+2R_2)\ Cext$ .....(4.3)

The frequency = 1/Total period = $1/0.693(R_1+2R_2)\ Cext$ ..... (4.4)

A frequency of 8Hz is selected. Also Cext is selected equal to 1μF.

To produce 50% duty cycle R_1 must be greater than 500Ω and $R_2 >> R_1$. 50% duty cycle means that charging time is equal to discharging time

By selecting $R_1 = 20k\Omega$ and substituting in equation 4.4,

$R_2 = 80k\Omega$

The value of resistor selected are

$R_1 = 20k\Omega$ and $R_2 = 100k\Omega$

4.3 RESETABLE AUDIO OSCILLATOR CIRCUIT DESIGN

It was realised from overall circuit diagram that the output pin Q of demultiplexer are fed into the resetable audio oscillator circuit. Since audio frequency range is between 20Hz – 20kHz, frequency of about 1kHz has been selected in the design, which was connected in the astable mode as shown in fig. 4.5.

Duty cycle = ON/T.P = t_2/T.P

Where

t_1 = charge time

t_2 = discharge time

Charge time = $0.693(R_3+R_4)C_2$

Discharge time = $0.693\ R_4C_2$

Frequency = $1/T.P = 1/0.693(R_3+2R_4)C_2$

$= 1.44/(R_3+2R_4)C_2$

To achieve a frequency of 1KHz, the following values of component were selected

$C_2 = 0.1\mu F$

$R_3 = 1k\Omega$

$R_4 = 6k\Omega$

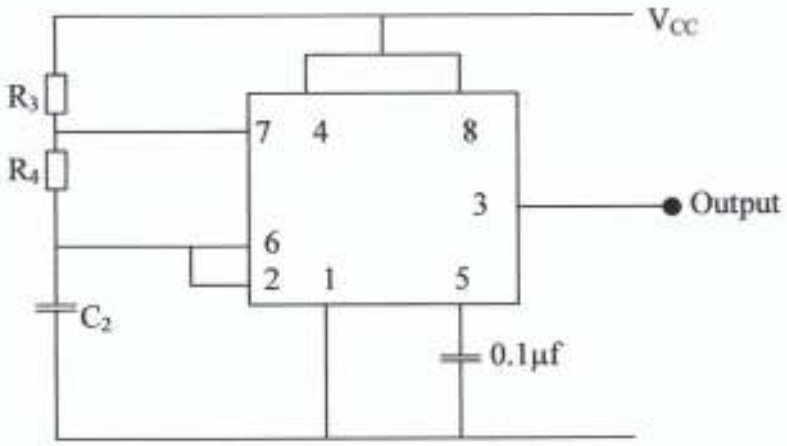


Fig 4.5:- Circuit Design for Resetable Audio Oscillator

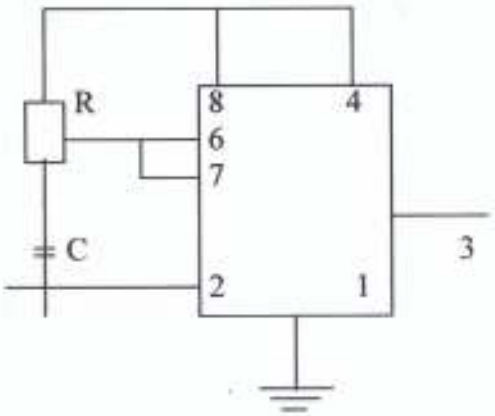


Fig 4.6:- 555 Configured for Monostable Operation

4.4 *DESIGN OF IC555 MULTIVIBRATOR IN ONE SHORT MODE*

As shown in fig. 4.6, 555 timer configured in monstable mode was used in pins 1 and 7 of 4 to 16 line decoder. Pins 2 and 7 were fed into the inlet valve and heater respectively to give a single pulse with a specified duration each time a special configured trigger pulsed is delivered to pin 2.

Mathematically, the time interval required for the capacitor to charge from 0 volt to 2Vcc/3 is given as

$2Vcc/3 = Vcc [(1-exp (-t/RC)]$ 4.5

$1/3 = exp (-t/RC)$ 4.6

$In\ 3 = t/RC$

Therefore on time is

$T = 1.1RC$

Let select $C = 10\ \mu f$

And period $T = 30$ sec.

From equation 4.6

$R = T/1.1C$

$= 30/1.1 \times 10^{-6} \times 10$

$= 3 \times 10^{6}$

The value of R was selected to be $3M\Omega$.

CHAPTER FIVE

5.1 DIGITAL COUNTER

Time sequencing and counting of events are all functions of which a digital circuit may be designed. These are function that can be realised using a digital counter. Like flip-flops, a counter can retain an output state after the input condition which brought about the state has been removed. While a flip-flop can occupy one of only two possible states, a counter can have many more than two states. In the case of a counter, the value of a state is expressed as a multidigital binary number, whose '1's and '0's are usually derived from the outputs of internal flip-flops that make up the counter.

Digital counters are usually made up of a cascaded interconnection of flip-flops. Any number of flip-flops may be involved in a counter, as demanded by counters application. Any counter whatever its function is provided with a "clock" input to which a digital pulse train can be applied. When the counter receives a clock pulse, it is caused to advance from its present state to the next state in the count sequence.

There are basically 2 types of counter, asynchronous and synchronous

5.1.1 ASYNCHRONOUS COUNTER

When the pulse to be counted applied at on end of the counter and the binary output can record a count of 0 to 1. When the count exceeds 1 (i.e. binary 2) then the stage must reset to 0 and a carry of 1 is transferred to the next stage. Similar conditions apply for the next stage in that it too can only record an output of 0 or 1 and to exceed this count will mean resetting the output to 0 and transferring the carry of 1 to the next stage and so on. Thus a

carry bit is seen to ripple-through the counter until the count is completed. For this reason asynchronous counters are often referred to as ripple-through counter.

5.1.2 SYNCHRONOUS COUNTER

In this case, clock pulses applied to each stage of the counter simultaneously. Problems encountered with ripple counter are caused by the accumulated flip-flop propagation delays which means the flip-flops do not all change state simultaneously in synchronism with the input pulses. These limitations can be overcome with the use of synchronous or parallel counter in which all the flip-flops are triggered simultaneously by the clock input pulses.

Synchronous counter can thus operate at a much higher input frequency than an asynchronous counter with same number of flip-flop. However synchronous counter requires more circuitry than the asynchronous counter.

5.2 DESIGN OF ASYNCHRONOUS (RIPPLE) COUNTER

In this project, an asynchronous mod 16 counter was used. It serves as an address input to the demultiplexer.

Fig 5.1 shows a 4-bit binary counter which was used in the design.

Its operation can be summarized thus:

(1) The clock pulses are applied only to the clock input of FFA. Thus FFA will toggle (change to its opposite state) each time the clock pulses make a negative (high to low) transition.

Note J=K=1 for all FFS

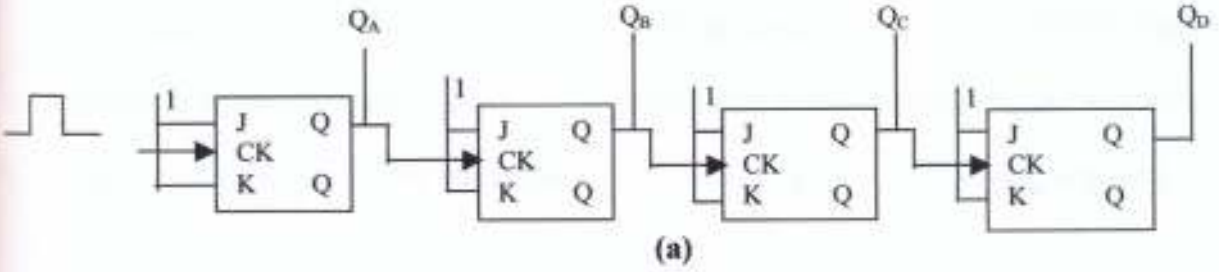
(2) The normal output of FFA will toggle each time a output goes from 1 to 0. Simultaneously FFC will toggle when B goes from 1 to 0 and FFD will toggle when C goes from 1 to 0.

(3) The Table 5.1a shows the sequence of binary states that the FFS will follow as clock pulses are continuously applied.

Since A,B,C,D represent a binary number, with D being the MSB and A LSB, the binary counting sequence from 0000 to 1111 is produced.

(4) After the 15^{th} clock pulse has occurred the counters FFS are in the 1111 condition. On the 16^{th} clock pulses, FFA goes from 1 to 0, which causes FFB to go from 1 to 0 and so on until the counter is in the 0000 state. In other words the counter has gone through one complete cycle (0000 through 1111).

The type of counter used in this project where each FF output serve as the clock input signal for the next FF is referred to as an asynchronous counter. This is because all the FFS do not change states in exact synchronism with the clock pulses. Only FFA responds to the Clock pulses. FFB has to wait for FFA to change state before it is toggle. FFC has to wait for FFB and so on. Thus there is a delay between the response of each FF

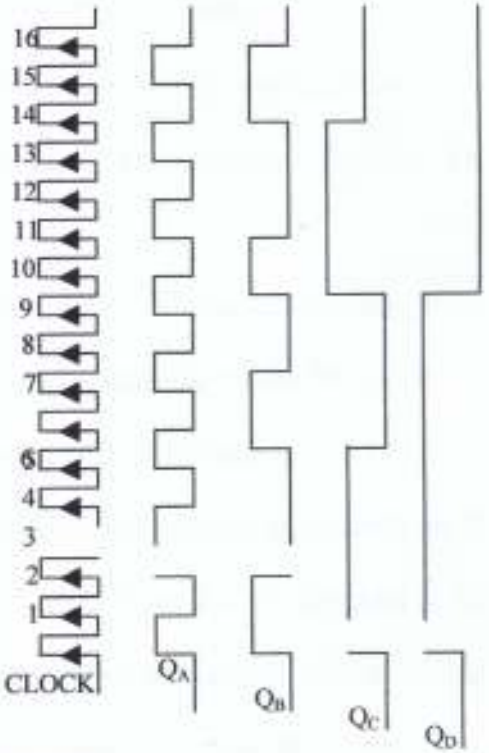


(a)

CK	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	1	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

(b)

Table 5.1a: Truth table of Mode 16 Binary Counter



(c)

Fig. 5.1 MOD 16 BINARY COUNTER

(a) CIRCUIT DIAGRAM **(c) TIMING DIAGRAM**

5.3 COUNTERS WITH MOD NUMBER LESS THAN 2^N (SN 7493)

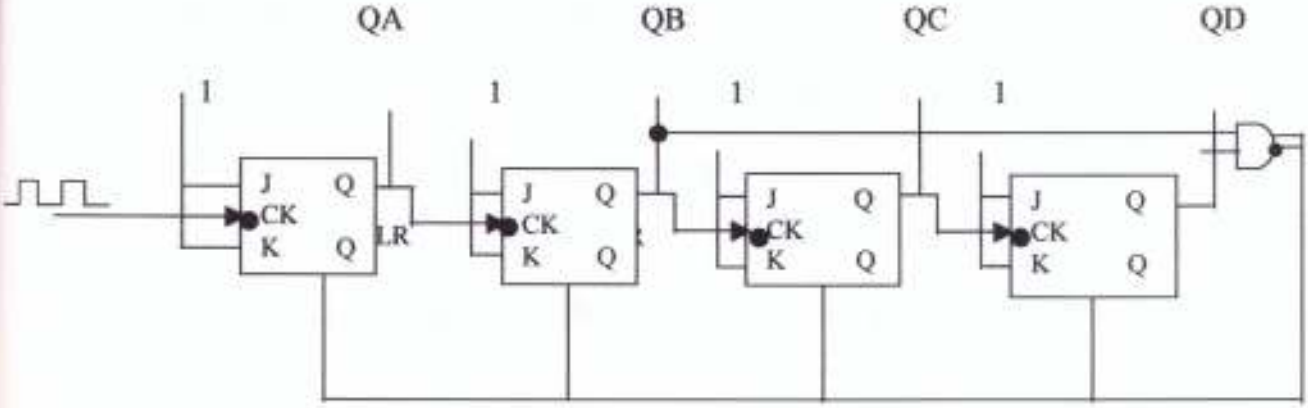
The basic ripple counter we just discussed is limited to MOD number that is equal to 2^N, where N is the number of FFS. Since the design also has to do with MOD 60 counter and decade counter, the basic counter can be modified to produce MOD number less than 2^N by allowing the counter to skip states that are normally not part of the counting sequence.

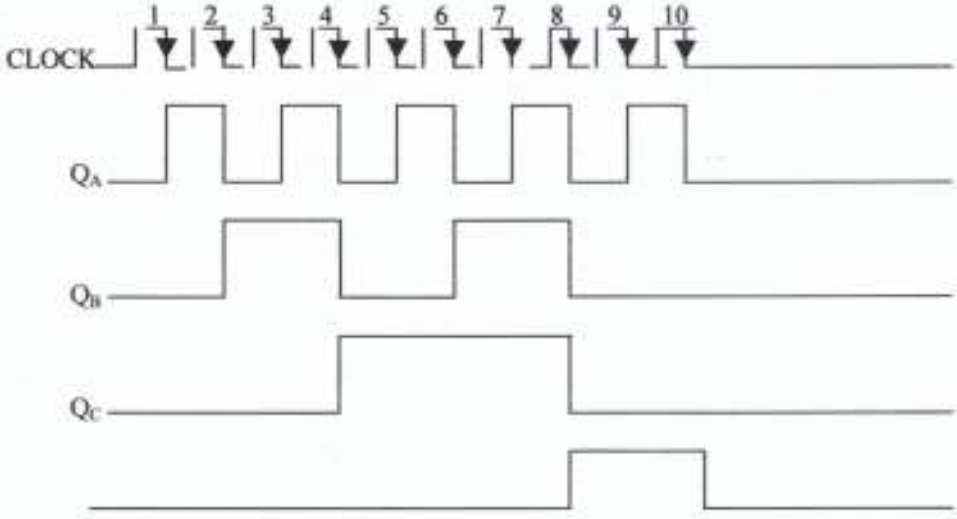
5.4 DESIGN OF MODULO 10 (OR DECADE) COUNTER (SN 7490)

In the design, modulo 10 counter is also used. Since three flip-flops give a count of 8 and four flip-flop give a count of 16 (2^4) then for a modulo 10 counter four flip-flops are necessary with external gating to modify the count.

The counting sequence is therefore shown in fig. 5.2(a). The counter counts from 0000 (Zero) to 1001 (Nine) and then recycle to 0000. It essentially skip 1010, 1011 to 1111 so that it only goes through nine different states, thus it is modulo 10 counter.

The simplest modification is to provide a NAND gate, with inputs from flip-flops B and D, to give an output to clear inputs as shown in fig 5.2(b). Since it is on the count of 10 (QA = 0, QB = 1, QC = 0, QD = 1) that B=D=1, then it is only on the count of 10 that a clear pulse is generated, and the output of the NAND gate going low will reset the counter. The flip-flop output waveform is as shown in fig 5.3c





CK	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

Table 5.2(a): Truth table Of a decade counter

Fig 5.2 (b)

Fig. 5.2 Asynchronous decade counter
(a) Circuit Diagram
(b) Timing Waveforms

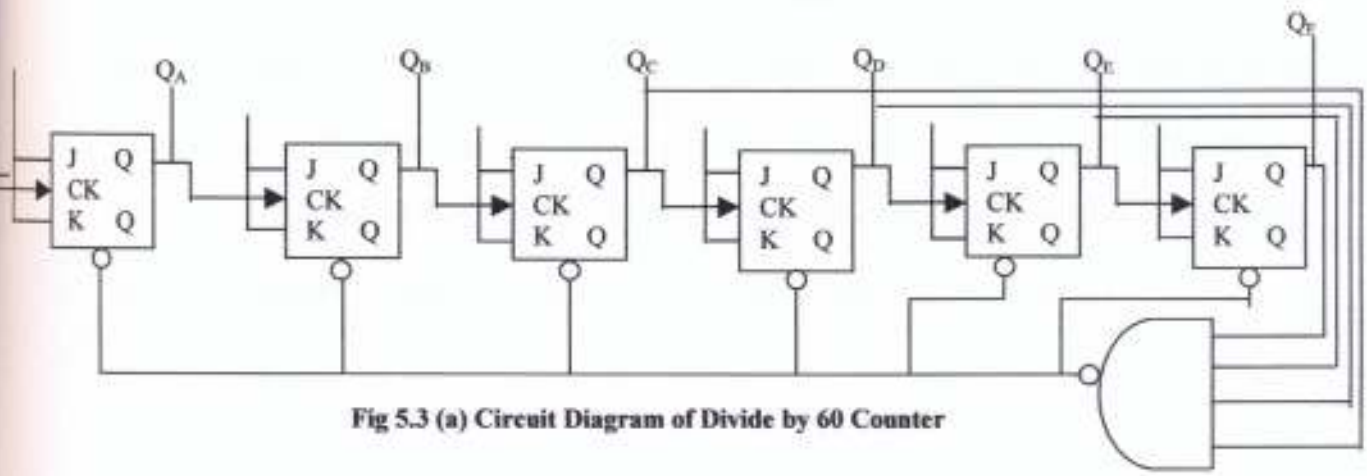


Fig 5.3 (a) Circuit Diagram of Divide by 60 Counter

5.5 *DESIGN OF MODULO 60 COUNTER*

The project was designed in such a way that the clock frequency obtained (from clock generator) is applied to the counter (i.e. divide by 60 counter). The clock frequency signal is 8Hz.

For a modulo 60 counter six flip-flops are necessary with external gating to modify the count.

i.e. $2^N \geq 60$

$2^5 = 32$, 5FFS will not be enough

$2^6 = 64$, so FFS would produce a counter that would count as high as 111111 = 64.

The counting sequence in this case is as shown in fig. 5.3. The counter counts from 000000 (zero) to 111011 (fifty nine) and then recycle to 000000. It essentially skip 111100 to 111111 so that it goes through fifty nine different states, thus it is modulo 60 counter.

A NAND gate with inputs from flip-flops C, D, E and F is provided to give an output to clear input as shown in fig 5.4a. Since it is on the count of 60 ($Q_A = 0$, $Q_B = 0$, $Q_C = 1$, $Q_D = 1$, $Q_E = 1$, $Q_F = 1$) that C=D=E=F=1, then it is only on the count of 60, that a clear pulse is generated, and the output of the NAND gate going low will reset the counter.

With reference to the project proper, the design was done in such a way that clock frequency signal is 8Hz. The flip-flop output waveform is such that waveform output A is 4kHz, B is 2Hz, C is 1Hz, D is 0.5Hz, E is 0.25Hz and F = 0.133Hz. Therefore, the output of flip-flop F has a frequency equal to the original clock frequency divided by 60. In general for any counter, the output from the last flip-flop divides the input clock frequency by the MOD number of counter i.e. MOD 60 counter is also called divide by 60 counter.

CK	F	E	D	C	B	A
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
4	0	0	0	1	0	0
5	0	0	0	1	0	1
6	0	0	0	1	1	0
7	0	0	0	1	1	1
8	0	0	1	0	0	0
9	0	0	1	0	0	1
10	0	0	1	0	1	0
11	0	0	1	0	1	1
12	0	0	1	1	0	0
13	0	0	1	1	0	1
14	0	0	1	1	1	0
15	0	0	1	1	1	1
16	0	1	0	0	0	0
17	0	1	0	0	0	1
18	0	1	0	0	1	0
19	0	1	0	0	1	1
20	0	1	0	1	0	0
21	0	1	0	1	0	1
22	0	1	0	1	1	0
23	0	1	0	1	1	1
24	0	1	1	0	0	0
25	0	1	1	0	0	1
26	0	1	1	0	1	0
27	0	1	1	0	1	1
28	0	1	1	1	0	0
29	0	1	1	1	0	1
30	0	1	1	1	1	0
31	0	1	1	1	1	1
32	1	0	0	0	0	0
33	1	0	0	0	0	1
34	1	0	0	0	1	0
35	1	0	0	0	1	1
36	1	0	0	1	0	0
37	1	0	0	1	0	1
38	1	0	0	1	1	0
39	1	0	0	1	1	1
40	1	0	1	0	0	0
41	1	0	1	0	0	1
42	1	0	1	0	1	0
43	1	0	1	0	1	1
44	1	0	1	1	0	0
45	1	0	1	1	0	1
46	1	0	1	1	1	0
47	1	0	1	1	1	1
48	1	1	0	0	0	0
49	1	1	0	0	0	1
50	1	1	0	0	1	0
51	1	1	0	0	1	1
52	1	1	0	1	0	0
53	1	1	0	1	0	1
54	1	1	0	1	1	0
55	1	1	0	1	1	1
56	1	1	1	0	0	0
57	1	1	1	0	0	1
58	1	1	1	0	1	0
59	1	1	1	0	1	1
60	0	0	0	0	0	0

Table 5.3: Truth Table of Modulo 60 Counter

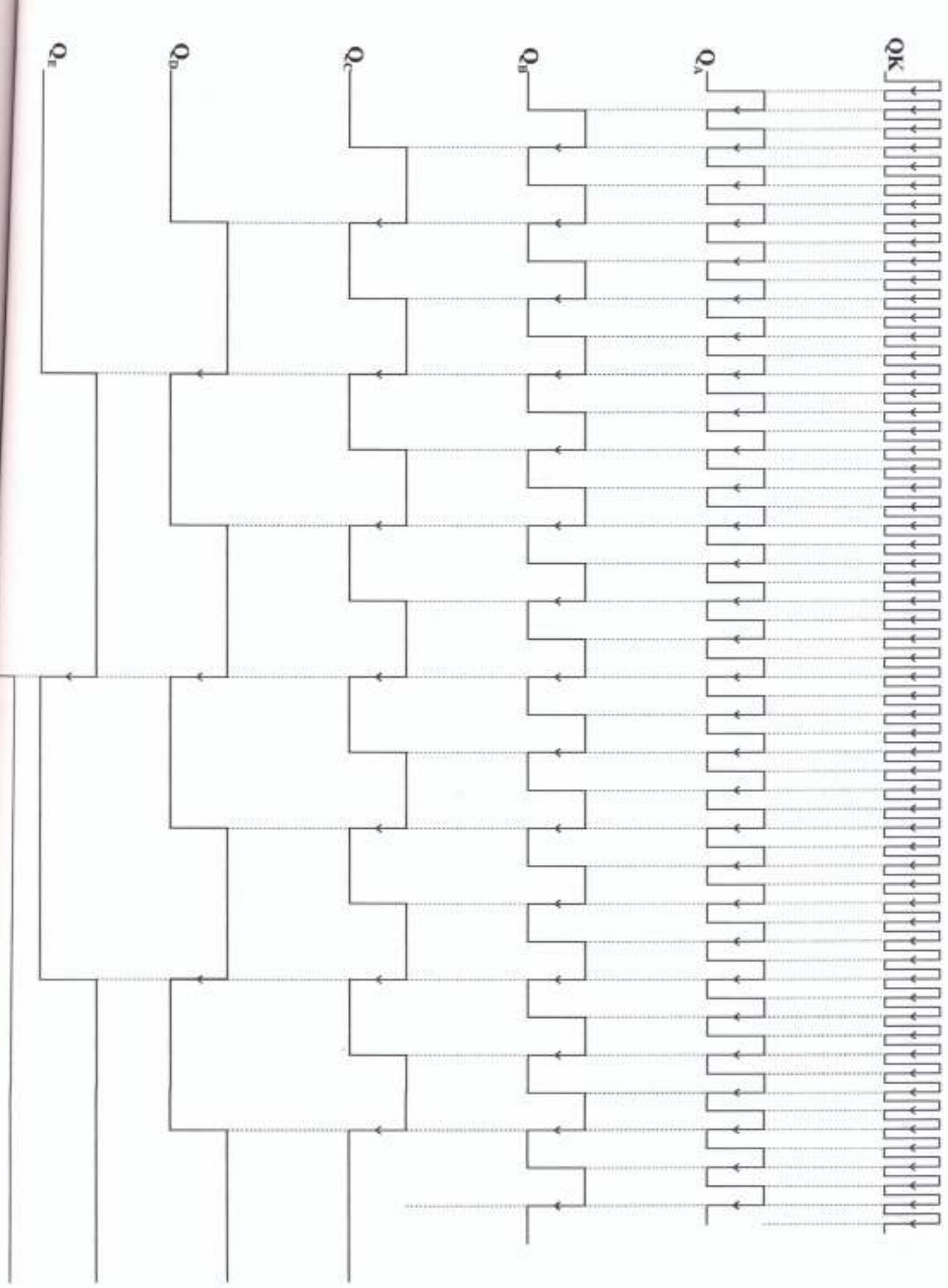


Fig. 5.4 TIMING WAVEFORM OF DIVIDED BY 60 COUNTER

5.6 DESIGN OF VARIABLE FREQUENCY DIVIDER

In this project, the output from the last MOD 60 counter serves as a clock of frequency 0.133Hz (7.5 sec) to variable frequency divider counter. In this case we can generate divide by 2, divide by 4, divide by 8, divide by 16 counters etc.

The variable frequency divider is a JK flip-flop that is connected in its toggle mode. It is a JK flip-flop connected in cascade as shown in fig 5.5.

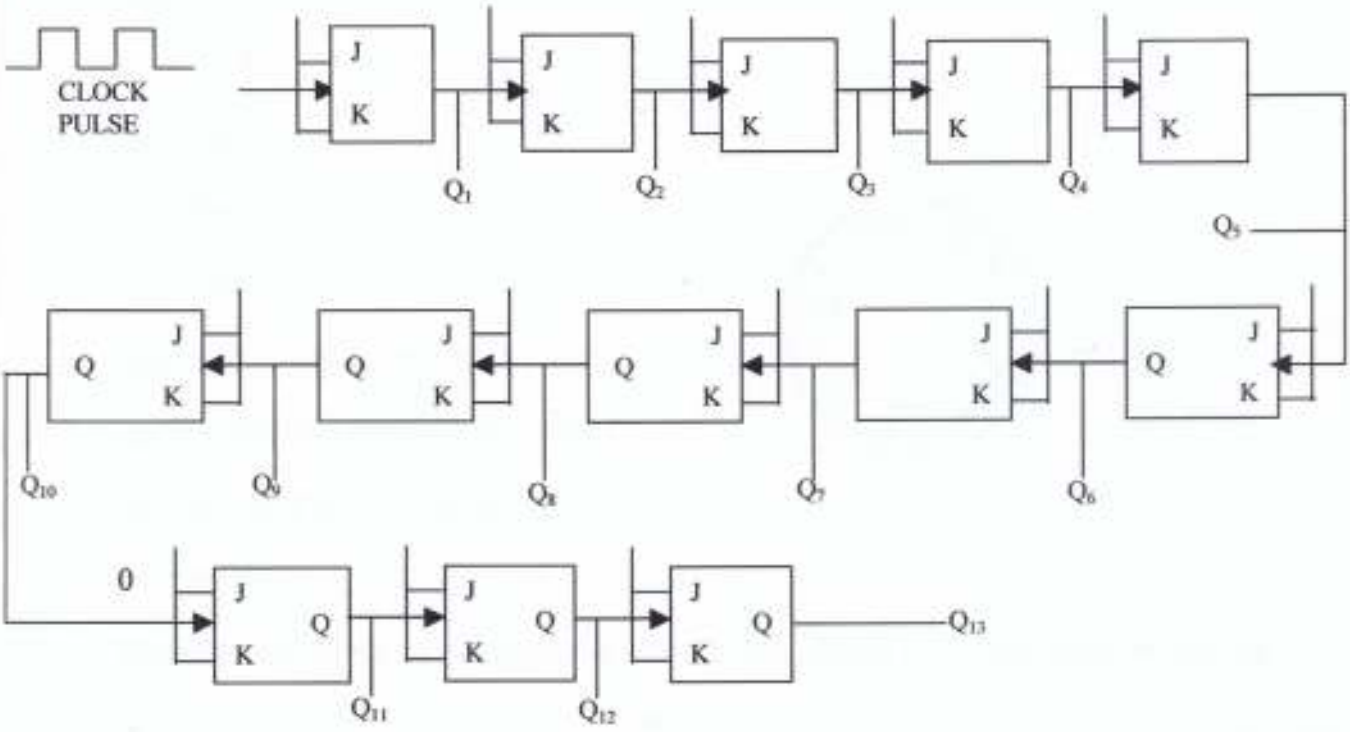


Fig 5.5 Circuit Diagram of Variable Frequency Divider

Each of the outputs is an exponential divider i.e. $Q_1 = 2^1$, $Q_2 = 2^2$, $Q_3 = 2^3$, $Q_4 = 2^4$, $Q_5 = 2^5$, $Q_6 = 2^6$, $Q_7 = 2^7$, $Q_8 = 2^8$, $Q_9 = 2^9$, $Q_{10} = 2^{10}$, $Q_{11} = 2^{11}$, $Q_{12} = 2^{12}$, $Q_{13} = 2^{13}$.

Note that frequency = 1/time

The output of frequency divider used are $Q_A = 2^1$, $Q_B = 2^2$, $Q_C = 2^3$, $Q_4 = 2^4$ with input frequency of 0.133Hz

Q_A = Fin/2

Q_B = Fin/4

Q_C = Fin/8

Q_D = Fin/16

Q_A = 0.133/2 Hz = 0.0667Hz =15sec

Q_B = 0.1333/4Hz = 0.03333Hz = 30sec

Q_C = 0.1333/8 Hz =0.01667Hz = 60sec

Q_D = 0.1333/16 Hz = 0.008333Hz = 120sec

Therefore the output of the multi frequency divider chosen are 15sec, 30sec, 60sec, and 120sec.

5.7 DESIGN OF 4 BY 1 MULTIPLEXER

The outputs from variable frequency divider are fed into a 4 by 1 multiplexer.

A multiplexer or data selector is a logic circuit that accepts several data inputs and allow only one of them at a time to get through to the output. The routine of the desire data input to the output is controlled by select input (Address input). The figure below shows a digital multiplexer

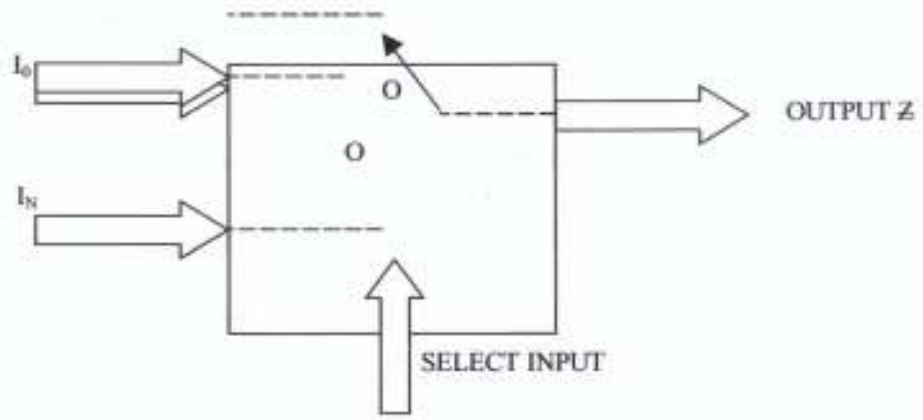


Fig 5.6 Functional Diagram of a Multiplexer

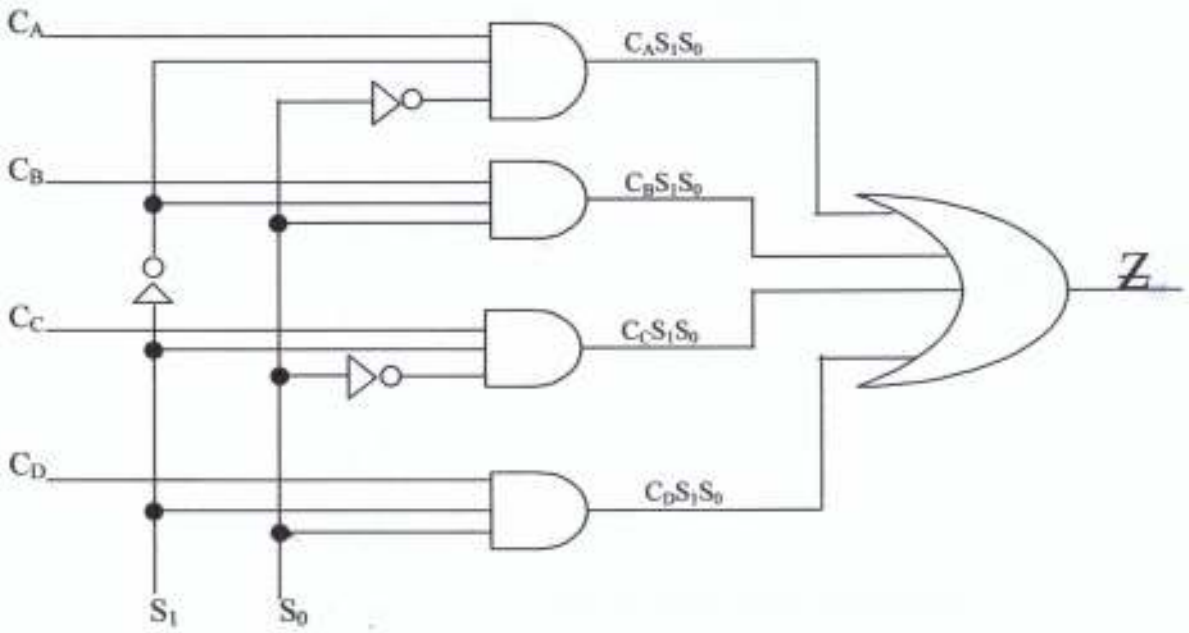


Fig 5.7 (a) Logic Circuitry for Four Input Multiplexer

The multiplexer acts like a digitally controlled multiposition switch in with the digital code applied to the select input controls which data input will be switched to the output e.g output Z will equal data input I_O for some particular select input codes; Z will equal I_1 for another particular select input codes and so on. Multiplexer therefore select 1 out of N-input data source and transmit the select data to a single output channel.

For the purpose of this project four input (4 by1) multiplexer was used. Fig 5.7 a shows the logic circuitry for a four input multiplexer with data input C_A, C_B, C_C and C_D and select inputs S_B and S_A

The Boolean expression for the output is Z = CAS1S0 + CBS1S0 + CCS1S0 + CDS1S0

Each data input is gated with a different combination of select input level. CA is gated with S1S0 so the CA will pass through its AND gate to output Z only when S1 = 0 and S0 = 0. The truth table in fig 5.7 b explain how the selection is achieved.

S_1	S_0	Output Q_X
0	0	C_A
0	1	C_B
1	0	C_C
1	1	C_D

Table 5.4 (b) Truth table for Four Input Multiplexer

C_A, C_B, C_C and C_D are inputs of the 4 to 1 multiplexer which are fed from Q_A, Q_B, Q_C and Q_D output of the variable frequency divider.

CHAPTER SIX

DESIGN CALCULATION AND OPERATION OF LOGIC CONTROL SYSTEM

This chapter deals extensively with the analog to digital conversion process of the control of the machine. The analysis of the design and operation of logic control microprocessor, programmable logic array and interface circuitry are fully discussed here. Fig. 6.2 shows the complete diagram of the logic control system.

6.1 LOGIC CONTROL MICROPROCESSOR

Modulo 16 binary counter and 16 to 1 Demultiplexer / 4 to 16 line Decoder are used as the logic control microprocessor.

A decoder generally is a logic circuit that converts an N-bit binary input code into M output line such that each output line will be activated by only one of the possible combination of inputs. Fig. 6.1 shows the general decoder diagram with N-input and M-output.

For each of these input combinations only one of the M-output will be active high, all other output are low. Many decoders are designed to produce active low outputs, where only the selected output is low while others are high.

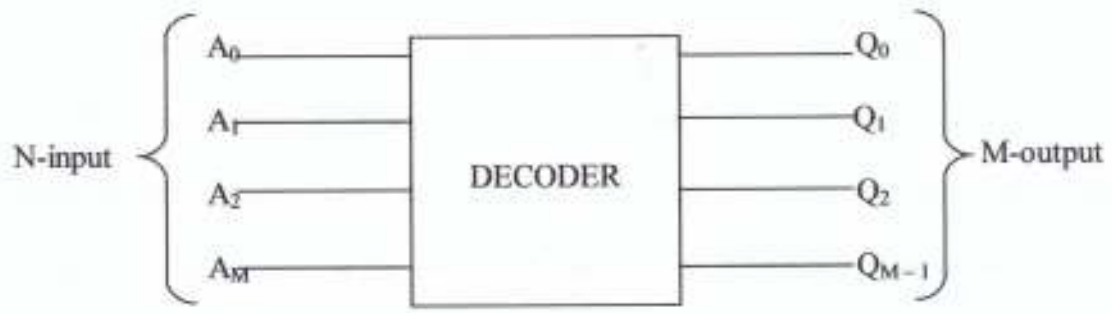


Fig. 6.1: General Decoder Diagram with N-input and M-output

Some decoders do not utilize all of the 2^N possible input codes but only certain ones e.g a BCD to decimal decoder has a 4-bit input code and ten output lines that correspond to the ten BCD code groups 0000 through 1001. Decoders of these types are often designed such that if any of unused codes are applied to the input, none of the output will be activated.

The decoder can be referred to in several ways. It can be called 3lines – to – 8line decoder because it has 3-input lines and 8-output lines. It could also be called a binary-to octal decoder this is because its 3bits binary input code can activate one of the eight (octal) outputs corresponding to that codes. It is also referred to as a 1-of-8 decoder because only 1 of the output is activated.

In this project, output Q_A, Q_B, Q_C, and Q_D of the modulo 16 binary counter are connected to the select input of the 4 to 16 line decoder and is used to select which output of the 4 to 16 decoder to be activated.

The 4 to 16 line decoder are active low device therefore an inverter is connected to each of the output of the decoder to make it an active high device.

When the 4 bit binary counter is counting from 0 to 15, each inverted output of the 4 to 16 line decoder is activated at each binary count.

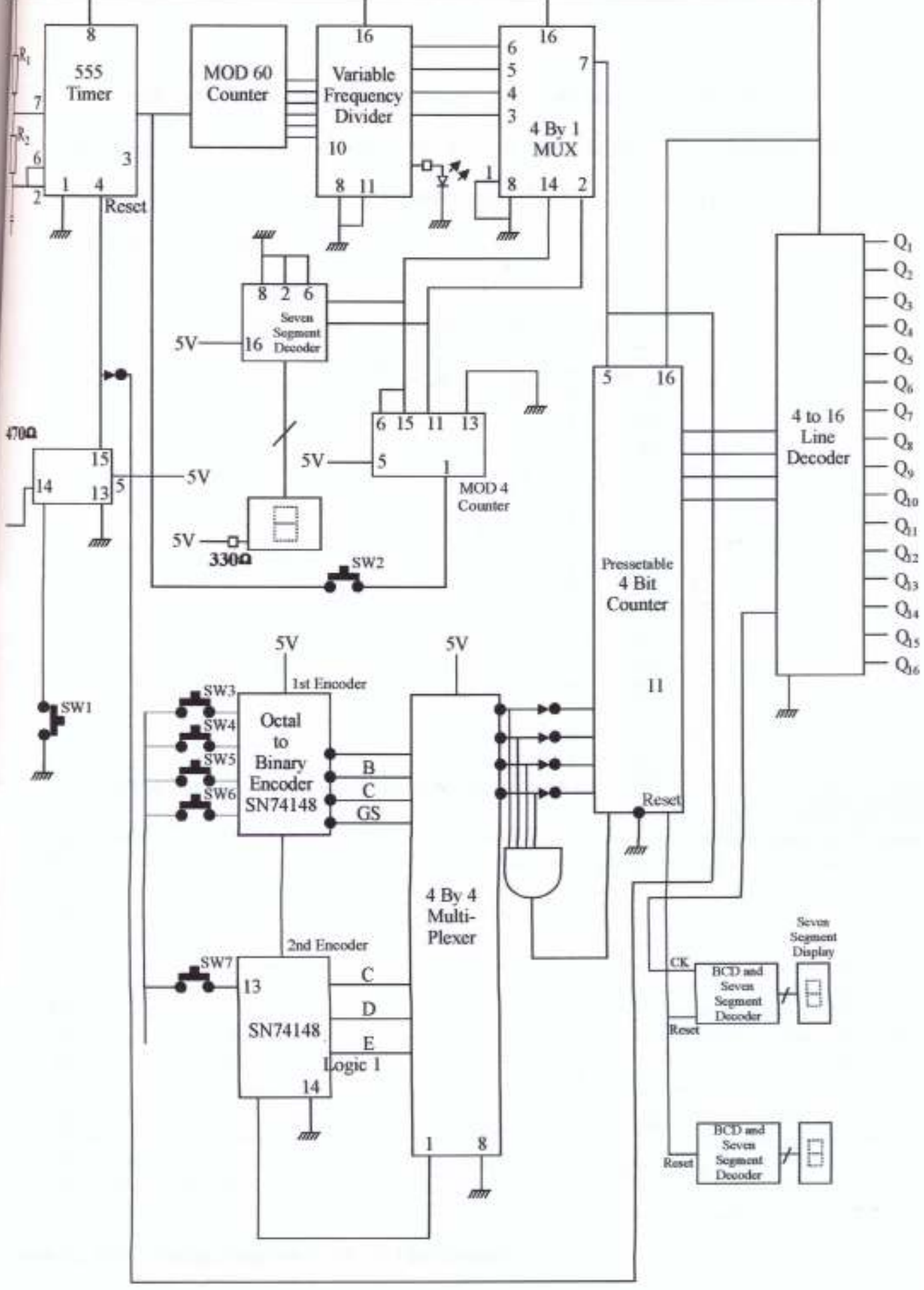


Fig. 6.2: Block Diagram of Logic Control Circuit

Table 6.1(a) shows the truth table while table 6.1(b) shows the timing diagram. The clock input of the modulo 16 counter is fed from the output of the 4 by 1. Multiplexer, this means that the total time to complete the decoding of the 16 lines is determined by the output of the 4 by 1 multiplexer.

Decimal Equivalent	Q_H	Q_G	Q_F	Q_E	4 to 16 line
	S_D	S_C	S_B	S_A	Decoder
0	0	0	0	0	Q_0
1	0	0	0	1	Q_1
2	0	0	1	0	Q_2
3	0	0	1	1	Q_3
4	0	1	0	0	Q_4
5	0	1	0	1	Q_5
6	0	1	1	0	Q_6
7	0	1	1	1	Q_7
8	1	0	0	0	Q_8
9	1	0	0	1	Q_9
10	1	0	1	0	Q_{10}
11	1	0	1	1	Q_{11}
12	1	1	0	0	Q_{12}
13	1	1	0	1	Q_{13}
14	1	1	1	0	Q_{14}
15	1	1	1	1	Q_{15}

Table 6.1 (a) :- Truth Table of 4-to16 Line Decoder

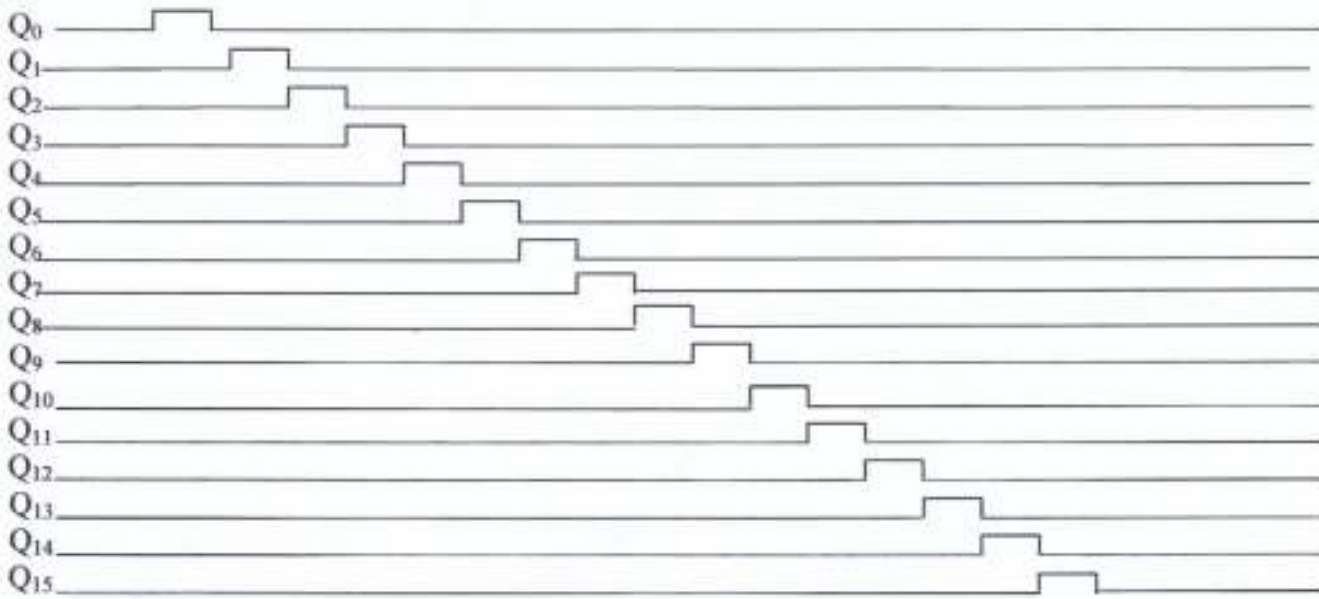


Table 6.1 (b):- Timing Diagram of 4 to 16 Line decoder

If C_A is routed to Q_M output of the 4 by 1 multiplexer, it means 15sec is used to clock the modulo 16 counter. It indicates that the total time that would take to complete the decoding of the 16 lines is

15sec x 16 = 240secs
i.e. 240sec = 240/60mins
= 4mins

Table 6.2 shows the time for decoding the 16 line for each output of the 4 by 1 multiplexer used to clock the modulo 16 counter.

Input of 4 by 1 MUX routed to Q_M	Q_M time (sec)	Decoder line	Total time taken (sec)	Total time (mins)
C_A	15	16	15x16 = 240	4mins
C_B	30	16	30x16 = 480	8mins
C_C	60	16	60x16 = 960	16mins
C_D	120	16	120x16 = 1920	32mins

Table 6.2 :- Truth Table for Decoding 16 Lines

6.2 *PROCESS INDICATOR SYSTEM*

There are two types of processes to be monitored viz:

(1) The type of cloth that is been washed.

(2) The set mode of the washing machine.

The type of cloth to be washed is controlled and monitored by using a modulo 4 counter output to feed a seven segment decoder and the select input of the 4 by 1 multiplexer.

The clock input of the modulo 4 counter is fed from Q_A of the variable frequency divider which gives $4H_Z$ (0.25 sec) via a normally open push button. When the push button is depressed, the counter advances from 0 through 11. The push button can be activated to set

modulo 4 counter to the counting mode the users need. *Table 6.3 shows the truth table of* modulo 4 counter.

Q_B	Q_A	Q_M
0	0	C_A
0	1	C_B
1	0	C_C
1	1	C_D

Table 6.3:- Truth Table of Modulo 4 Counter

The type of cloth to be washed dictates the total time taken to complete the decoding of the 16 lines of the 4 to 16 line decoder and the modulo 16 counter which is used to control the decoding cycle is controlled from the output of the 4 by 1 multiplexer output. It can be seen that when the multiplexer output is routed to 15sec input it gives the lowest decoding time cycle and when routed to 120sec it gives the maximum decoding time cycle. Therefore the selection of the input of the 4 by 1 multiplexer to be routed to the output gives the type of fabric to be washed.

The output of the modulo 4 is fed to a seven segment decoder which decodes the binary output to give its decimal equivalent on the seven segment display and at the same time the output is fed to the select input of the 4 by 1 multiplexer.

Table 6.4 shows how the modulo 4 counter is used to select the output of the 4 by 1 multiplexer and also the decoding by seven segment decoder.

Q_B S_I	Q_A S_O	Q_M	Decoding time Q_M	Seven segment no display
0	0	C_A	15sec	0
0	1	C_B	30sec	1
1	0	C_C	60sec	2
1	1	C_D	120sec	3

Table 6.4:- Selection of 4 by 1 mux

The seven segment number displayed can be interpreted for the use of the user to determine which type of cloth is to be washed as shown in 6.5

Seven segment display	Type of cloth to be washed
0	Very light material
1	Light material
2	Heavy material
3	Very heavy material

Table 6.5: Type of Cloth to be washed with Equivalent segment

The process of monitoring the mode in which the washing machine is achieved by using two modulo 10 counter connected is cascade to count from 0 to 15. The outputs of the two cascade modulo 10 counter are connected to two seven segment decoder which decodes the binary counting and the seven segment display to display the equivalent decimal number.

The display is used to monitor which output of the 4 to 16 line decoder is been activated because the output Q_m of the 4 by 1 multiplexer is simultaneously applied to the cascade counter and to the clock input of the modulo 16 counter which is used as to select which output of the 4 to 16 line decoder is to be activated. Table 6.6 shows how this is achieved.

Operation of 2-cascade BCD counter:- If BCD counter is to be used to count beyond 9 digit (binary 1001), two or more counters have to be cascaded. In this design, two cascaded BCD counter were used. In this case, all the counters are initially set at 0000 by applying a reset pulse to all counters simultaneously. The condition of the two counters is now:

0000	0000
Tens	Units

For 9-clock pulse, the unit counter has an output state of 1001. On the tenth clock pulse, the MSB of the unit counter changes from 1 to 0. The high to low transition trigger the "tens" counter and units counter returns to 0000 as shown in this table 6.6

0001	000
Tens	Units

The counter counts until it reaches 15 clock pulse when the condition of the counter is now

0001	0101
Tens	Units

In general, after the First 9-clock pulse, as ten further pulses arrive, the unit counter advances to 1001 again and on the next pulse, the ten counter read 0010. Thus in 99 clock pulses the BCD counter reads

1001	1001
Tens	Units

The maximum number of clock pulses which can be counted by these two cascaded BCD counter is 99.

	OUTPUT OF MOD 16 COUNTER				OUTPUT OF 2- CASCADES BCD COUNTER								4-16 line Decoder Output
Seven segment display	QH	QG	QF	QE	TENS COUNTER				UNITS COUNTER				
	S_D	S_C	S_B	S_A	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	
00	0	0	0	0	0	0	0	0	0	0	0	0	Q_0
01	0	0	0	1	0	0	0	0	0	0	0	1	Q_1
02	0	0	1	0	0	0	0	0	0	0	1	0	Q_2
03	0	0	1	1	0	0	0	0	0	0	1	1	Q_3
04	0	1	0	0	0	0	0	0	0	1	0	0	Q_4
05	0	1	0	1	0	0	0	0	0	1	0	1	Q_5
06	0	1	1	0	0	0	0	0	0	1	1	0	Q_6
07	0	1	1	1	0	0	0	0	0	1	1	1	Q_7
08	1	0	0	0	0	0	0	0	1	0	0	0	Q_8
09	1	0	0	1	0	0	0	0	1	0	0	1	Q_9
10	1	0	1	0	0	0	0	1	0	0	0	0	Q_{10}
11	1	0	1	1	0	0	0	1	0	0	0	1	Q_{11}
12	1	1	0	0	0	0	0	1	0	0	1	0	Q_{12}
13	1	1	0	1	0	0	0	1	0	0	1	1	Q_{13}
14	1	1	1	0	0	0	0	1	0	1	0	0	Q_{14}
15	1	1	1	1	0	0	0	1	0	1	0	1	Q_{15}

Table 6.6:- Selection of Output of 4-16 Line Decoder with it necessary Display

6.3 PROGRAMMABLE LOGIC ARRAY (PLA)

The PLA is an arrangement of logic gates which has been selected to accept the output of the 4 to 16 line decoder and produce an output according to pre-planned sequential movement.

To fully understand the PLA circuitry, the operation of the washing machine should be fully understood.

In the washing chamber, the following are needed

- Inlet valve – which allows water in
- Motor with 2 speeds and with both clockwise and anticlockwise movement.
- Outlet valve which allows water out
- Low heating mode by the heater
- High heating mode by the heater

The table 6.7 shows the sequence of operation of the washing machine.

The letter P with subscript 0 to 7 represents action at the chamber

P0 = Inlet valve

P_1 = Outlet valve

P_2 = Low heating mode

P_3 = High heating mode

P_4 = Low motor speed with clockwise rotation

P_5 = Low motor speed with anticlockwise rotation

P_6 = Motor at high speed

In the table 6.7, a dash line (-) at each of the process or action shows that the system is idle (not in operation) while a 1 at each of the process shows that the action comes on. The table also shows the mode in which the washing machine is and also which of the output of the 4 to 16 line decoder is activated. In this case let us assume the following

D = Output of 4 to 16 line decoder activated

M = Mode of the washing machine

S = Seven segment to show the process indicator

ACTION AT THE WASHING CHAMBER							PROCESS MONITORING SYSTEMS		
P_0	P_1	P_2	P_3	P_4	P_5	P_6	D	M	S
-	-	-	-	-	-	-	Q_0	NOP	00
1	-	-	-	-	-	-	Q_1	K_1	01
-	-	1	-	1	-	-	Q_2	K_2	02
-	-	1	-	1	-	-	Q_3	K_2	03
-	-	-	-	-	-	-	Q_4	NOP	04
-	-	1	-	-	1	-	Q_5	K_2	05
-	1	-	-	-	-	-	Q_6	K_3	06
1	-	-	-	-	-	-	Q_7	K_1	07
-	-	-	-	1	-	-	Q_8	K_4	08
-	-	-	-	1	-	-	Q_9	K_4	09
-	-	-	-	-	-	-	Q_{10}	NOP	10
-	-	-	-	-	1	-	Q_{11}	K_4	11
-	1	-	-	-	-	-	Q_{12}	K_3	12
-	1	-	-	-	-	1	Q_{13}	K_5	13
-	1	-	-	-	-	1	Q_{14}	K_5	14
-	-	-	-	-	-	-	Q_{15}	AOP	15

Table 6.7:- Washing Machine's Process Control

AOP = Audio Oscillation Operation

NOP = No Operation

K_1 = Water allowed in

K_2 = Washing mode

K_3 = Water allowed out

K_4 = Rinsing mode

K_5 = Spinning mode

Fig. 6.3 shows how PLA is arranged to obtain the process controller shown in table 6.7

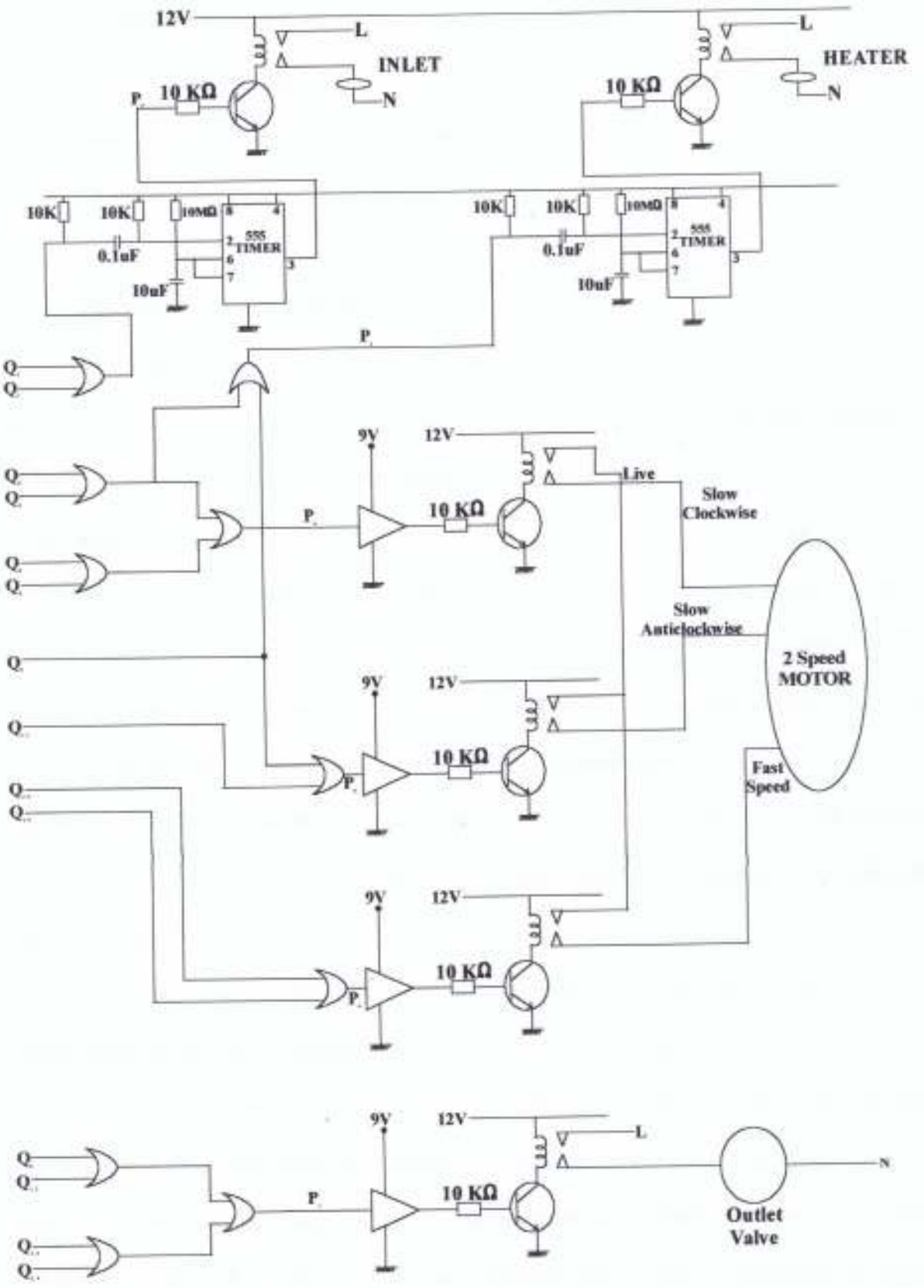


Fig. 6.3 PLA/INTERPHASE DECODING CIRCUITS

6.4 *INTERFACE CIRCUIT UNIT*

In this unit, electromechanical part of the washing machine is taken into consideration. Fig. 6.4 shows the interface circuit connection.

The relays, the valves, the pump motor and electric motor are discussed here

6.4.1 *THE RELAY AND VALVES*

No exposition of switching devices would be complete without including electromagnetic switches or relays. A switch whose lever is operated by electromagnet is called by that name. The contact arrangements are the same as for switches and the same symbols are often used.

Many different types of special purpose relays such as polarised relays, a.c relays, sensitive relays exist; but we will concentrate only on the general purpose d.c relay. This type of relay operates when the current through its coil exceeds a certain value (called the operate current) and remain operated until the current diminishes below another value called the release current. The time it takes for the contact to close after the application of the operation current ranges from a few milliseconds to several hundred milliseconds. An important characteristics of the operation of a relay is contact stagger. When a relay operates, the contacts do not open or close instantaneously and so there may be a delay of several milliseconds between the operation of two contact of the same relay.

The symbol used for a relay coil is the "coil" symbol shown in fig. 6.4a. The most common method of controlling the operation of a relay is shown in fig 6.4b. Here a contact is placed in senses with the relay coil and a battery. When the contact is closed, current flows through the relay coil and the relay operates. Occasionally, a relay is controlled by a shunt

contact as in fig 6.4c. When the contact is closed, it places a very low impedance path in parallel with the relay coil and the current from the battery flows through the shunt path rather than through the relay coil, preventing the relay from operating. When the contacts are open, then it operates provided that the value of R is chosen properly.

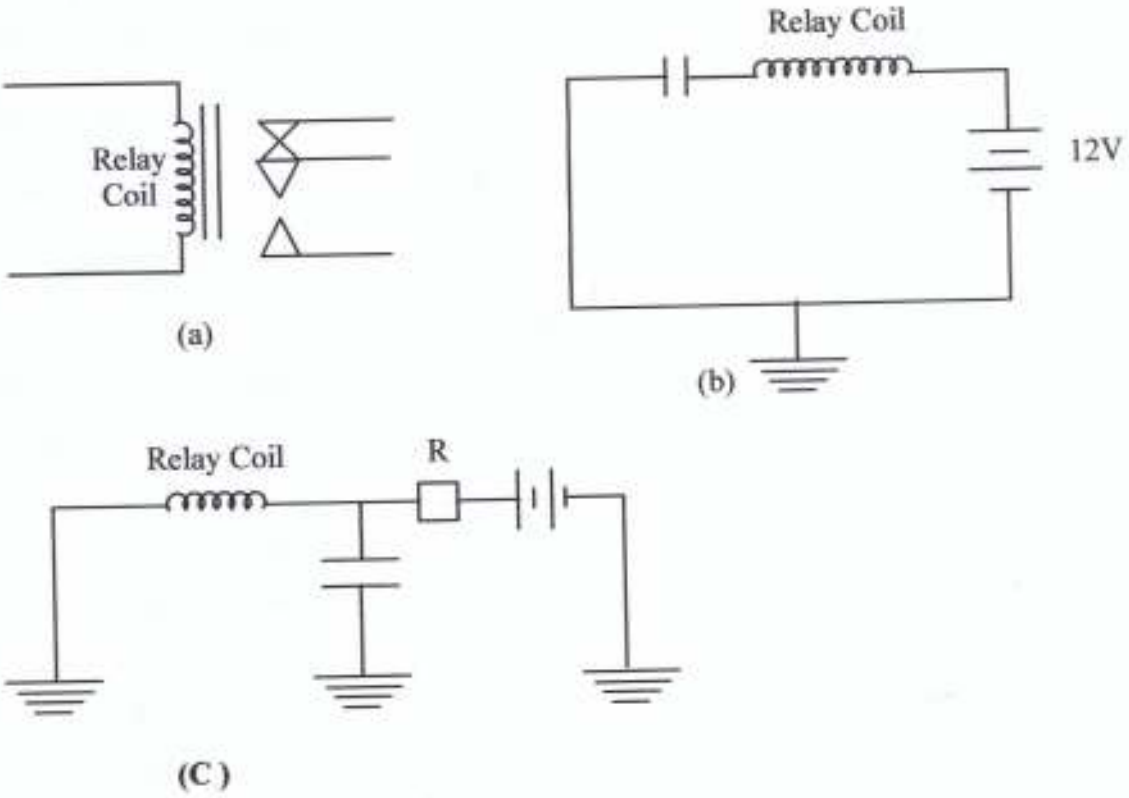


Fig 6.4: Relay Connections

In this project, the relay that is available in the market is the 12V d.c operated relay coil which can handle up to 10A and can switch 220V main supply.

The reasons for the choice of this relay is that there are two high wattage consuming devices. They are the industrial heater and the 1.2 horse power motor

Mathematically, Power = Voltage X Current

Heater wattage = 1000W

Voltage = 220V

$I = P/V = 1000/220$ 6.1

$= 4.55A$ for the heater

1 horse power = 746W

1.2 h.p = 746X1.2

= 895.2W

Supply Voltage = 220V

Current through the motor

$I = 895.2/220$

$I = 4.07A$ 6.2

Since these are the two major consuming device, therefore the relay contact can carry the main supply current.

6.4.2 *TRANSISTOR SWITCHING OPERATION AND ITS OPERATING POINT*

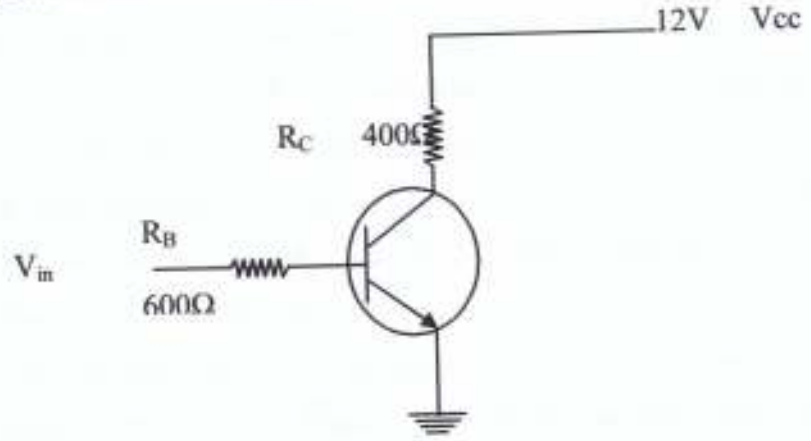
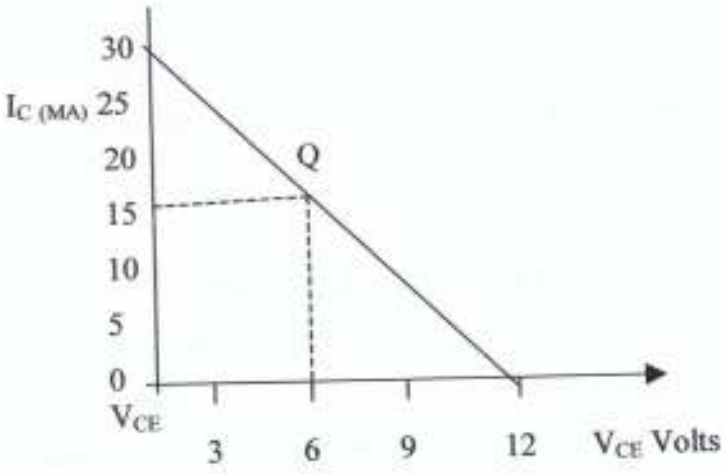


Fig 6.5: Transistor Switching and Biasing



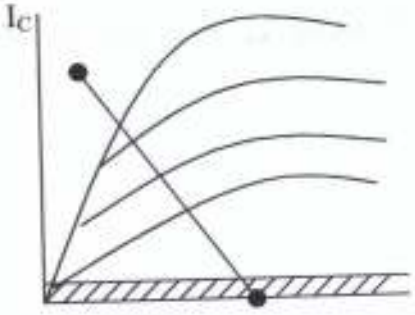


Fig. 6.6:- D.C Load line

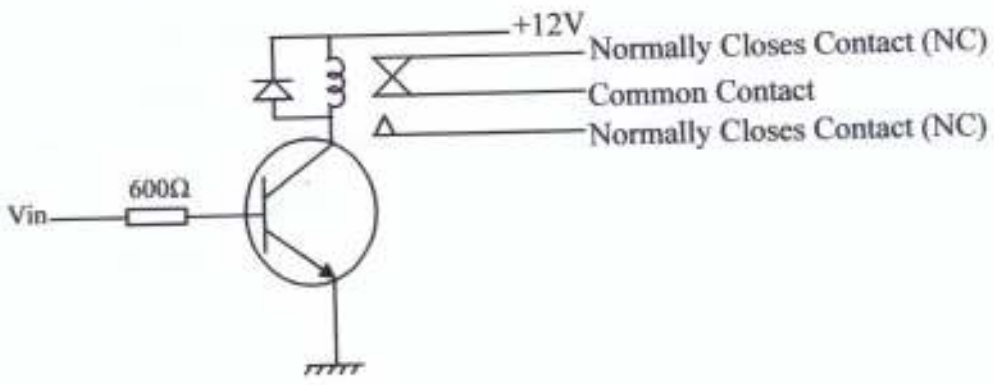


Fig 6.7: Transistor as a Switch

When a voltage is applied to the base of the transistor, the transistor start conducting and the current will flow in the relay coil. When current is sent through the winding, a force is produced thereby energising the coil and the contacts. In this case a normally closed contact (NC) will open while normally open contact (NO) will closed. The force developed by the electromagnet between the coil and the contact is a function of the current through the winding, the number of turns in the winding, the core and the width of the air gap.

When the current through the relay winding is removed, the transistor is non-conducting and the magnetic force which tending to hold the air gap closed disappear immediately except for a decaying eddy current in the core material. Under this condition the contact would return to the normal position because the coil would be de-energised due to non-flow of current in the relay coil.

In this interface unit, all a.c loads are connected to the normally open contacts of the relay while the main is connected to the common terminal.

6.4.3 VOLTAGE OPERATED VALVE

The mains supply is applied to the valve this causes electromagnetic induction and thereby pulls the valve cover to open the passage for water and when the mains supply is disconnected, the valve's cover is pulled back to its original position to close the passage for water.

The resistance of the valve coil is 960Ω, therefore the current consumption of the valve coil is

$$I = V/R = 220V/960\Omega$$

$$= 0.229A$$

:- The power consumed $= I^2R$ 6.9

$$= (0.229)^2 \times 960\Omega$$

$$= 50Watt$$

6.5 *ELECTRIC MOTOR AND PUMP MOTOR*

Such motors which are designed to operate from a single-phase supply are manufactured in a large number of types to perform a wide variety of useful services in homes, factories, offices, workshops and in business establishment etc. Since the performance requirements of the various applications differ so widely, the motor-manufacturing industry has developed many different types of such motors, each being design to meet specific demands.

Single phase motors may be classified under depending on their construction and method of starting

(i) Induction motors (split phase, Capacitor and shaded pole)

(ii) Repulsion motors (sometime called inductive series motor)

(iii) A.C series motor

(iv) Unexcited synchronous motors

In this case, single phase capacitor start induction-run motor was used as the electric motor in the project. Constructionally, this motor is more or less, similar to a polyphase induction motor except that its stator is provided with a single phase winding. When fed from a single-phase supply, its stator winding produces a flux (or field) which is only alternate i.e. one which alternates along one space axis only. It is not a synchronously revolving (or rotating) flux as the case of a 2- or 3-phase supply. Now an alternating or pulsating flux acting on a stationary squirrel-cage rotor cannot produce rotation (only a revolving flux can). That is why a single-phase motor is not self-starting.

To overcome this drawback and make the motor self starting. It is temporarily converted into a two-phase motor during starting period. For this purpose, the stator of a single-phase motor is provided with on extra winding known as starting (or auxiliary) winding addition to the main or running winding. The two windings are spaced 90^0 electrically apart and are connected in parallel across the single-phase supply as shown in fig. 6.9.

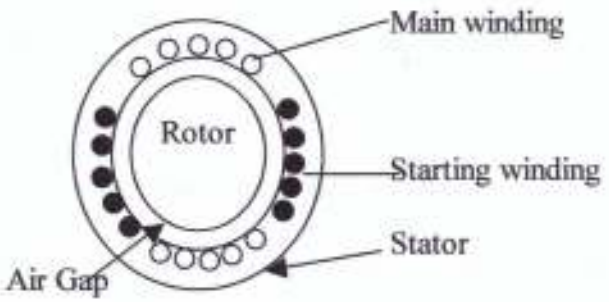


Fig. 6.8:- Single-phase induction motor with main and starting winding separately

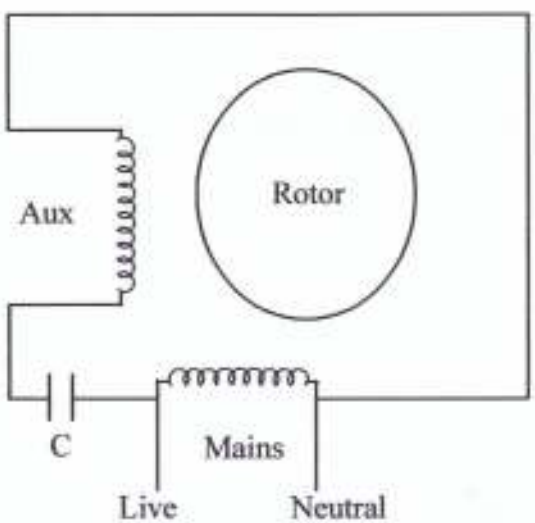


Fig. 6.9: Electric Motor having Auxiliary and Mains Windings Connected via a Capacitor

Another problem is how to produce two phase. This problem can be solved by connecting the mains supply to the auxiliary winding via a capacitor as shown in fig. 6.9

The capacitor produces a lagging phase due to its characteristics. This lagging phase now becomes the pseudo phase which now compliment the mains supply and thus produce rotational field that can now rotate the rotor.

Without the auxiliary winding connection via the capacitor, the rotor will not rotate obvious when main supply is applied to the mains winding by slightly rotating the rotor the mechanic rotates continously, but on load the rotor may not rotate, thus burning out the coil due to large current flow in the mains winding when the motor is not rotating.

The direction of rotation of the rotor depends largely on the connection of the auxilliary winding, if the auxiliary winding is connected via the capacitor produces a lagging phase which is positive in direction and the motor rotates clockwisely.

When the auxiliary windings are connected via the capacitor as shown in fig. 6.10c. The capacitor produces a lagging phase which is negative in direction and the motor rotates anticlockwisely.

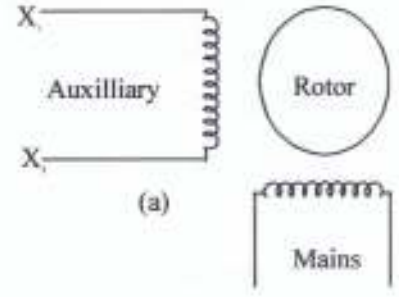
Fig 6.10:-

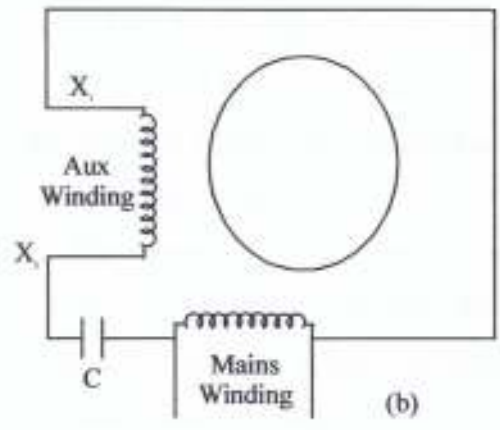
(a) Arrangement for electric motor connection

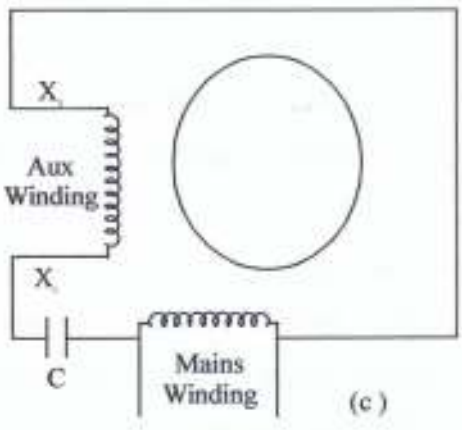
(b) Electric motor connected in clockwise direction

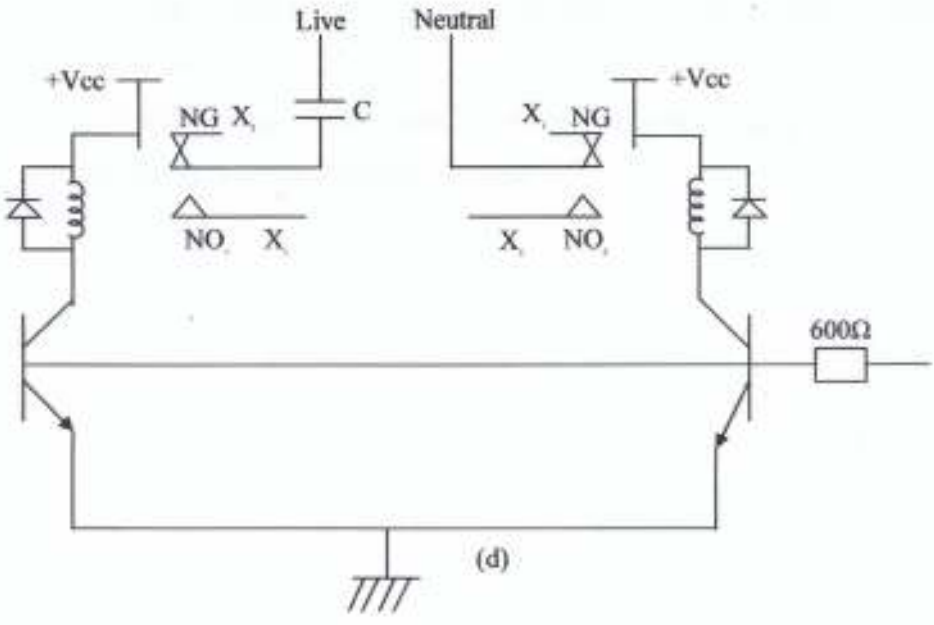
(c) Electric motor connected in anticlockwise direction

(d) Two transistorized control relay for interchange the auxiliary winding with the starting winding









Two transistorized controlled relays are used so as to effect the clockwise and anticlockwise motion of motor by interchanging the auxiliary coil of the motor with the mains supply and the starting capacitor.

This arrangement is shown in fig 6.10 a,b,c,d. Fig 6.10 (a) shows the coil of auxilliary winding and the main winding, taking cognizance of the auxiliary windings connection ends X_1 and X_2. Fig 6.10 (b) shows the arrangement for the clockwise rotation of the motor's rotor. Fig 6.10 (c) shows the arrangement for the anticlockwise rotation of the rotor. Fig 6.10 (d) shows two transistorized control relay been used to interchanging the auxiliary windings with the starting capacitor.

When the input logic to the base is zero NC_1 and NC_2 make contacts with their common and the auxiliary winding is connected as shown fig 6.10 (b) thereby making the motor to rotate in the clockwise direction.

If the input logic to the base is logic1 NO_1 and NO_2 make contacts with their common and the auxiliary winding is connected as shown in fig 6.10 (c) making the motor to rotate in anticlockwise direction.

The motor is two-speed type as shown in fig. 6.11 speed can be changed by changing the number of poles in the winding for which purpose two separate running windings are placed in the slots of the stator, one being 6-pole winding and the other, 8-pole winding. The double action has two contact points on the 'start' side and one on the 'run' side. The motor will always start on high speed irrespective of whether the speed switch is on the 'high' or 'low' contact (Theraja and Theraja 1994). If speed switch is on 'low', then as soon as the motor comes up to speed, the switch

(a) cuts out the starting winding and low-speed running winding

(b) cuts on the high-speed running winding

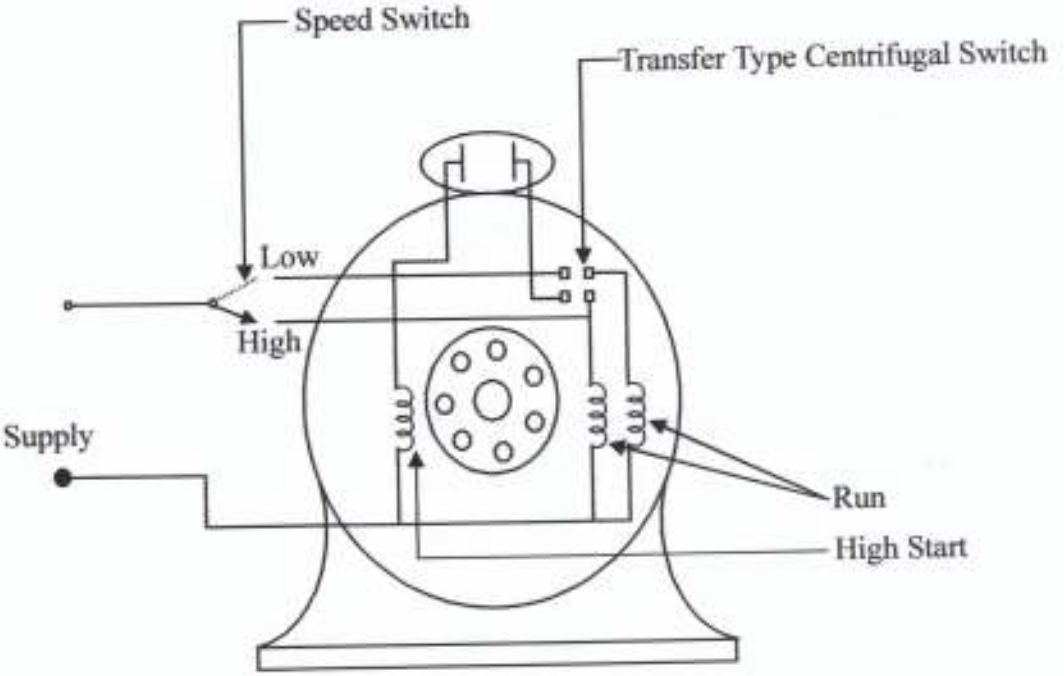


Fig 6.11: Connection of Two-Speed Type of Capacitor Start Motor

The heater is submerged so as to reduce the effect of an electric shock

The inlet and outlet valves are mains voltage operated valves. Their valves have a coil that can work directly with the 220V main supply.

The table 6.8 shows how the outputs of the PLA circuit is connected into the interface circuits.

PLA output	Interface
P_0	Inlet Valve
P_1	Outlet Valve
P_2	Low heating mode
P_3	High heating mode
P_4	Low motor speed with clockwise rotation
P_5	Low motor speed with anticlockwise rotation
P_6	Motor at high speed

Table 6.8:- Interface Circuits Outputs.

6.6 ENCODER AND PRESET STAGE

The system can be preset by the use of octal to binary encoder, dual 4 by 4 multiplexer and pressettable 4 bit up/down counter.

6.6.1 ENCODER

The purpose of the encoder in this design is to produce binary output of the input.

Inputs are wired through the switches to the ground potential. The octal to binary encoder has 8 possible outputs which represent all possible combination of 3-bit.

In the design of this project 2 octal to binary encoders had been cascaded to give 0 to 15 binary count. When a switch is depressed in the first encoder, pin 15 will be high and pin 5 of he 2^{nd} encoder will also be high, thus deactivate the 2^{nd} encoder. This will appear at the input of multiplexer as shown in fig. 6.13. The processes which were preset are pins 1, 2, 6, 8 and 13 of the output of 4 to 16 line decoder. In this case the system can be called back to repeat such process. This is done by the use of switches 3, 4, 5, 6 and 7.

Immediately SW 7 is pressed, second encoder is activated this makes pins 5 and 15 to be high which deactivate first encoder and binary equivalent of the second encoder is display to the input of the multiplexer. The encoder also incorporate an additional output labeled key rollover (kRo). This output goes low when more than one key is depressed at the same time it informs the circuit that the encoded output word is not valid and should be ignored.

6.6.2 DUAL 4 BY 4 MULTIPLEXER

At a particular time a multiplexer selects in one of many inputs to be transferred to one output.

In the design as shown in fig. 6.13. There is data select input depending on the value of these select input, the corresponding data input is transferred to the output. At a time when select input is zero, all the data input in 1st encoder are transferred to the output and also when S = 1 the data input in the 2nd encoder are transferred to the output.

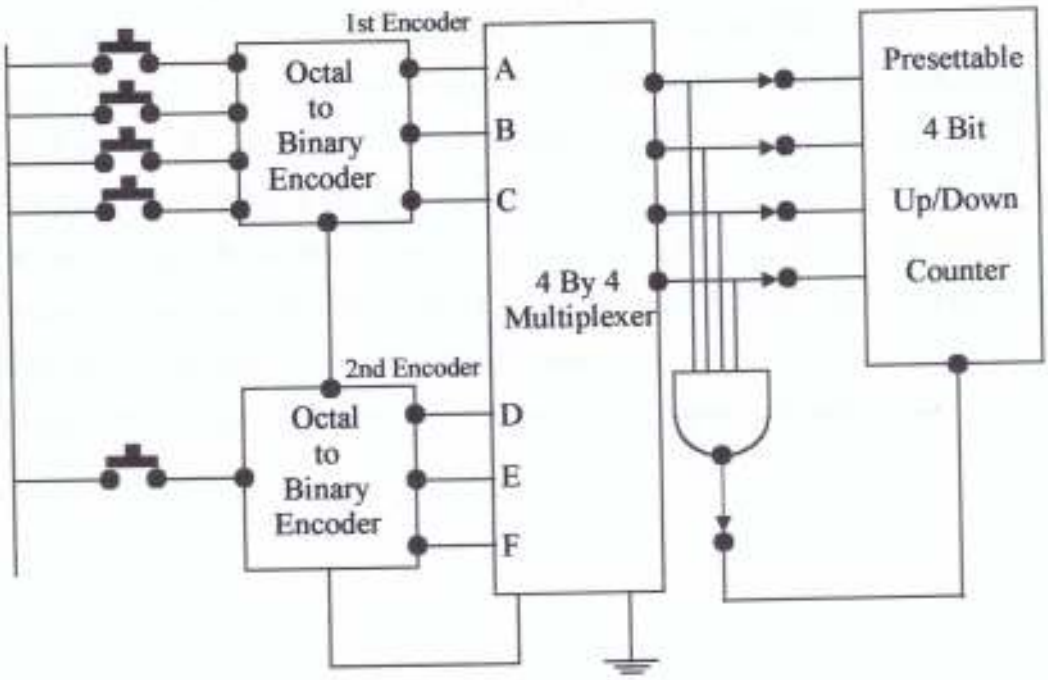


Fig. 6.13: Encoder / Preset Stage

6.6.3 PRESETTABLE 4 BIT UP/DOWN COUNTER

Preset is a process of shortening the count sequence of a particular counter by presetting it to be a non zero numbers. In this project, output of dual 4 by 4 multiplexer is passed through the inverter before applied to the presettable up/down counter this is because the chip (SN 74157 multiplexer) is an active low device which has to be inverted to have logical 1 into the input of the counter moreover, output of the multiplexer is also applied to Hexa inverter buffer. If is to be known that Hexa inverter buffer is provided with 4 input and the output is loaded into the counter. The load input L1, l2, L3 and L4 as shown in fig. 6.13 are used to preset the counter to any desired value.

At initial stage the inputs to the counter are normally low and all the inputs to the Hexa inverter are high and this makes pin 11, to be low and this will deactivate the counter. Immediately any of the inputs is low, the Hexa inverter.

Output will be high and the counter will be reset to any desired value.

CHAPTER SEVEN

DESIGN AND CONSTRUCTIONAL CONSIDERATIONS

The design of any electronic equipment required the knowledge of the basic principle of components and other materials used to construct equipment concerned. It is of importance to knows the exact estimate value of components and type of materials to be used to give satisfactory operation of the system.

The component cost and the availability of material and other major factors that cannot be ruled out were put into consideration since reliability of any electronic equipment depends on the quality of the material used to construct the equipment. The design and constructional aspect is based on the factor enumerated above.

The cost benefit analysis of the cost of production and increase in capability of the present design over the conventional one in the market indicates a tremendous improvement in term of efficiency and cost of production.

The controller was designed and constructed in such a way that the device can be programmed to determine the type of fabrics to be washed (which is determined by the user) and display the code for the fabric type and this selection actually determine time taken to wash the selected fabric.

Also selection of integrated circuit chip (IC) used depends on the type of job to be performed e.g TC4040 (I.C) was used as 4 multi frequency divider which aimed at selecting time alloted for each fabrics. SN74154 (IC) was used as 4 to 16 line decoder which is used as a logic control microprocessor which controlled the programmable logic array.

In carrying out the constructional aspect there must be availability of power in the laboratory working bench for soldering and testing the output of the soldered component on the oscilloscope.

7.1 DESIGN CRITERIA

For an efficient performance of the system the design of the system must fulfill some of the following requirements.

(i) Very frequent starting and stopping should be made possible without any harm on the system.

(ii) The system must be able to operate with load whose parameter vary widely

(iii) The system should be self-starting at press of start push button without any need for auxiliary equipment

(iv) The system must have sufficient tolerance to accommodate disturbances or fluctuations in the input power supply.

(v) The system must be able to deliver rated power within 10% limit of the design output frequency.

7.2 CONSTRUCTIONAL DETAILS AND PRACTICAL CONSIDERATION

The construction was done in the laboratory.

The whole system was arranged in 4 blocks. The digital control/ PLA unit, interface unit power supply and display unit.

7.2.1 CONSTRUCTION/ASSEMBLY

For proper appreciation of electronics that is the practical aspect must be carefully carried out, since the circuit designed will fail to perform the required function if the construction is badly done.

To ensure a good construction model the following steps were carried out

- Circuit layout drawing
- Circuit layout
- Soldering

It is worth noting that the following basic tools were used during the construction which include

- Long nose pliers
- Screw driver
- Soldering iron
- Vero board

(i.) Circuit Drawing:- With the help of the circuit diagram the component layout was produced on a breadboard sheet. Aæter the layout drawing, this was transferred to the Vero board.

(ii.) **Circuit Layout:-** The layout of the circuit component was carried out after confirming the functionally of all the components required for construction. The Vero board was cleaned with smooth sandpaper to remove likely dirt on the copper strip to the Vero board.

The laying of the component was made in line with the circuit diagram and drawing. There are two major factors to consider when laying out the wiring of power supply. First care must be taken to avoid any excessive lead inductance, which would prevent proper circuit performance. Also good rule is to maintain small spacing between the wire carrying heavy current to and from any part of the equipment.

The layout should be planned to minimize unnecessary coupling in the circuit. The power supply equipment should be layout and planned to minimized the length of the wire, this will result in low inductance as well as low wiring space and consequently reduce losses of improved regulation.

(iii.) **Soldering:-** The system was constructed by soldering it inside the Vero board. During soldering the tip of the soldering iron was cleaned and the components to be soldered were also cleaned and "tinned" by melting a thin smooth layer of liquid solder over the surface to be soldered to ensure good soldered joint.

Also component to be soldered together were held firmly and extra care were taken to that the components were tightly held while the solder is hardening since the solder may crystalline and create a very bad quality joint.

After the construction has bee done the equipment is neatly packed and mourled on existing washing machine.

7.3 TESTING AND RELIABILITY

The project was tested after completion in the Electronics laboratory of the Polytechnic, Ibadan. The voltages measured at the terminal of the Power Supply are 12V, 9V and 5Volts d.c.

Load Regulation Test: Load regulation can be defined as the change in output voltage for a given change in Load Current. It can be expressed as percentage change in output from No-Load (N.L) to Full-Load (F.L) as follows:

Load Regulation = $[(V_{NL} - V_{FL} / V_{FL}) \times 100\%]$

(Floyd 1990)

Therefore with the system set to a voltage of 27volts,

The Full-Load output Voltage V_{FL} = 23V.

:- The Load Regulation = $[(27 - 23.0 / 23.0) \times 100\%]$

= 0.17%

Thereafter, to confirm its reliability, the system was tested for about four different times. Table 7.1 shows the reading obtained.

	Decoding Time for each mode (sec)	Decoder Line	Total Time taken (sec)	Total Time (Mins)
Reading Expected	15	16	240	4.00
	30	16	480	8.00
	60	16	960	16.00
	120	16	1920	32.00
1st Reading Measured	14	16	224	3.73
	29	16	464	7.73
	59	16	944	15.73
	119	16	1904	31.73
2nd Reading measured	14.5	16	232	3.87
	29	16	464	7.73
	58	16	928	15.47
	119	16	1904	31.73
3rd Reading Measured	15	16	240	4.00
	29	16	464	7.73
	59	16	944	15.73
	120	16	1920	32.00
4th Reading Measured	14	16	224	3.73
	29	16	464	7.73
	59	16	944	15.73
	119	16	1904	31.73

It can be seen that the disparity between the expected reading and measured reading is not significant so it can be concluded that the system is reliable.

Also Test such as Load Regulation test was carried out in order to determine the suitability or efficiency of the system. It was found that load regulation of the system is 0.19. This shows that the workability or efficiency of the system is high.

7.4 BILL OF ENGINEERING MEASUREMENT AND ESTIMATION

A. Power Supply Stage

PART NO	DESCRIPTION	QUANTITY	UNIT ₦ PRICE	TOTAL ₦ AMOUNT
(1) 220V/30V a.c	Step-down Transformer	1	400:00	400:00
(2) IN400	Bridge Rectifier	1	250:00	250:00
(3) 6070μf	Capacitor	1	50:00	50:00
(4) 4.7KΩ	1/2 Watt Resistor	2	5:00	10:00
(5) LM7805	5V Monolithic regulator	1	60:00	60:00
(6) Lm 7809	9V Monolithic regulator	1	60:00	60:00
(7) LM7812	12V Monolithic regulator	1	60:00	60:00
(8) 12V, 9v	Zener diodes	20	20:00	40:00
(9) D313	Power transistor	2	60:00	120:00
	TOTAL			1050:00

B. Digital Control / PLA Unit

PART NO	DESCRIPTION	QUANTITY	UNIT ₦ PRICE	TOTAL ₦ AMOUNT
(1) NE 555	Oscillator	3	50	150
(2) TC 4040	Multi-modulo Counter	1	150	150
(3) SN 7476	Dual JK FF	2	150	300

(4) SN74153	4 By 1 Multiplexer	1	200	200
(5) SN74193	Presettable 4-bit up/down binary counter	1	300	300
(6) SN74157	Dual 4 by 4 Multiplexer	1	300	300
(7) SN74148	Octal to binary Encoder	2	200	400
(8) SN7420	Dual 4-input NAND gate	1	150	150
(9) SN74154	4to 16 line Decoder	1	1000	1000
(10) SN7432	Quad 2-input OR gate	3	150	450
(11) TL4050	TTL to CMOS Buffer	1	300	300
(12) 330Ω 470Ω	1/4 Watt Resistor	4	5	20
(13) 27KΩ, 1.5KΩ	1/4 Watt Resistor	2	5	10
	TOTAL			₦3,730

C. Interface Unit

PART NO	DESCRIPTION	QUANTITY	UNIT ₦ PRICE	TOTAL ₦ AMOUNT
(1) Relay	Electromechanical device	6	150	900
(2) SN7404	Hex Inverter Buffer	4	150	600
(3) C1815	Switching Transistor	6	10	60
(4) Contractor	Switching Relay	2	1000	2000
(5) 10KΩ	Resistor	12	5	60
	TOTAL			₦3,620

D. Display Unit

PART NO	DESCRIPTION	QUANTITY	UNIT ₦ PRICE	TOTAL ₦ AMOUNT
(1) SN7447	Seven segment Decoder	3	300	900
(2) SN7490	Decade Counter	2	200	400

(3) Seven segment display	Arrays of LEDS	3	150	450
(4) GREEN LED	Light Emitting Diode	1	5	5
(5) RED LED	Light Emitting Diode	1	5	5
	TOTAL			₦1,760

Others Unclassified

PART NO	DESCRIPTION	QUANTITY	UNIT ₦ PRICE	TOTAL ₦ AMOUNT
(1) 2 h.p motor	2 Speed motor	1	2000	2,000
(2) PCB	Printed Circuit Board	4		3,650
(3) Washer		1	8,000	8,000
	TOTAL			₦13,650

A.	Power Supply Stage	1,050
B.	Digital Control / PLA unit	3,730
C.	Interface Unit	3,620
D.	Display Unit	1,760
E.	Other Unclassified	13,650
GRAND TOTAL		₦23,810

The total cost of the device is twenty three thousand eight hundred and ten Naira only.

CHAPTER EIGHT

CONCLUSION AND RECOMMENDATION

The washing machine's controller designed and built has the property of displaying the mode in which the machine is and can also repeat certain process by the presettable counter. The flexibility of the controller is such that its decoding time can be varied depending on the type of fabrics and dirtiness of the cloth.

The execution of the project had not been very easy but very challenging as it had given more exposure to the use and principle of operation of more semiconductor devices. To achieve the desired objective all efforts were made both theoretically and practically in form of consulting relevant books and spending hours in some places like going to University College Hospital, Ibadan in understudying their industrial washing machine's operation and construction.

However, one of the major hindrances in this project is sourcing for the right component to use to give satisfactory operation. For example when the interphase was first tested, it was observed that the relays were not operating satisfactorily and spikes were generated. With the introduction of TTL to CMOS buffer (TC 4050) the problem was totally ameliorated.

The cost of the controller is cheaper and lower compared to the imported ones. Mass production of this type will help to conserve the necessary scarce foreign currencies in the country.

RECOMMENDATION

The school, through the department, should help students in securing components and instruments needed for projects. Since there is no good books in the library, most of the books used for the project were bought. It is thereby recommended that the school Library should relate more to the departments to know the books they really need, and that newer editions of old best-selling books (like The Art of Electronics - Horowitz and Hill) be procured.

For further researches on this project, I will like to recommend that such thing as remote control of the machine through the use of Computer be included. This will enable users with access to computer to be able to Control the washing machine at remote location.

Lastly, I will like to recommend that provision of funds and incentives for research into the institution of higher learning should be made available by the federal government. Also the design and construction of project, training of workers and public enlightenment must be put in place, so that Nigeria can be more involved in the global village in the twenty first century.

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A1

APPENDIX A

This manual provides information and instruction concerning this digital controller for the washing machine of size 4kg capacity.

It provides information regarding operation maintenance and fault finding of the device

A.2.

DATA

LOAD
MAXIMUM DRY WEIGHT — 4KG POLYESTER/COTTON ON SYNTHETIC

DIMENSION

BREADTH: 58CM

WIDTH: 46CM

HEIGHT: 78CM

CAGE SIZE

LENGTH: 50CM

DIAMETER: 26CM

TECHNICAL SPECIFICATION

- POWER REQUIREMENTS
- AC 220V –240V 50/60 H2
- AMBIENT TEMPERATURE RANGE

(1) $20^{O}C$ to $80^{O}c$ for the heater

(2) $0^{O}C$ to $55^{O}C$ for the integrated

- POWER CONSUMPTION

(1) AT very light material - 275 W/hr

(2) AT very heavy material - 2400 W/hr

- PROTECTIONS

  AC Fused Plug 13A

READ OUT:- Seven segment display

WEIGHT

NETT 60kg

GROSS (INCLUDING WATER AND WORK) 67kg

CAGE SPEED

WASH 38 R.P.M

EXTRACT :- 700 R.P.M.

A4 **FEATURES AND FACILITIES**

-PROCESS CONTROL MONITORING

The introduction of the double seven segment displays to indicate the mode in which the machine is operating enable the user to monitor the washing process.

AUDIO FACILITY

The availability of audio tone that signifies the end of operation gives the user the enable opportunity to attend to other things while the machine is washing.

FABRIC SELECTION

The availability of the push button gives the user the opportunity to program the machine by displaying the code needed for the fabric type

SPINNING / EXTRACT

The spinning effect of the machine in the machines chamber is to remove considerable amount of moisture from the material that is been washed

FUSED PLUG WITH INDICATOR

The fused plug serve as a means of protection for the equipment and the indicator light enable the user aware of presence of main.

OPERATION PROCEDURE

-Place the machine on the floor and make sure it has a high stability .

-Attach a hose-pipe to the inlet value and then to the tank

-Attach a hose-pipe to the outlet pump motor and then to the gutter.

-Plug the machine to the supply mains and switch it ON.

-Ensure that the double seven segment- display displays digits OO

-Press the push bottom and select the type of material to be washed.

-Open the detergent basin and pour in the detergent and the bleach.

-Put on the system by pressing the ON bottom

-Observe that green light emitting diode comes ON –this shown that the machine is ON.

-Observe the process indicator, double seven segment display number from OO to 15 during the machine Operation.

-Note the audio sound at the end of operation.

PROCESS INDICATOR

There are two types of indicator; one single seven segment display and double seven segmen display: The single seven segment displays the type of material to be washed. The doubl seven segment displays the mode of washing machine.

SINGLE DISPLAY

- very light material
- light material
- Heavy material
- Very heavy material

DOUBLE SEGMENT DISPLAY

00 N0 Operation

01 Inlet value Opens

02 Low heater and motor moving clockwise

03 Low heater and motor moving chokiest

04 No operation

05 Low heater and motor moving anticlockwise

06 Water inlet

07 Water inlet

08 Low heater with motor moving clockwise

09 Low heater with motor moving clockwise

10 No operation

11 Low heater with motor moving anticlockwise

12 Water outlet

13 High heating mode with motor at high speed

14 High heating mode with motor high speed

15 Audio signal generator.

MODES OF WASHING MACHINE

Water allowed in 01 and 07

Water allowed out 06 and 12

Washing mode 02 to 05

Rinsing mode 08 to 11

Spinning/Extract mode 13 to 14

Alarm.

NOTES ON FAULT TRACING

Source of the fault to the circuit diagram appropriate reference to the diagram.

The control circuit of the machines have been kept as simple as possible consistent with the required functioning of the machine .

Faultfinding is essentially a logical process, and much time can be saved by checking out control circuit in logical sequence.

The following pages attempt to give some guidance in tracing of faults that may arise in the course of the life of the machine.

FAULT TRACING

FAULT	POSSIBLE CAUSE	REMEDY
(1) Machine will not start when switched from start to "WASH".	Door safety relay not operating	Relay burnt out. Replace Relay
	No supply voltage on control circuit.	Check for blown fuse Quick check if supply voltage is okay.
(2) Load wetted at the end of Spin/Extract	Leaking water inlet valve	Strip and clean. Replace if damaged
(3) Water does not enter machine	Main supply shut off.	Check and restore main supply
	Fault on water/inlet valve.	Check water valve for operation
	No main water.	
	Fault switch on water control	Examine and replace faulty control.
(4) Drain/outlet valve remains open during WASH.	No voltage to drain outlet valve.	Using circuit diagram check through drain circuit for continuity until fault is located.
(5) Double seven segment does not display 00 at start.	Contact not properly made.	Press the start botton again.
(6) Water does not go out of the chamber.	Blockage in the water channel.	Unscrew the pump space and check for any blockage of water.
(7) Control running indicator light ON chamber does not move.	Fault demultiplexer (IC7)	Replace
(8) Outlet/Drain light "OUT" But drain open when it should be closed.	Drain valve defective mechanical defect inside drain valve casing.	Repair or Replace Dismantle and Refit.
(9) No light at the 13Amps Plug.	Fuse blown.	Replace the fused of the plug.

PRECAUTIONS

- Make sure the equipment is firmly connected to earth so as to safe guard the equipment from lightning.
- To help ensure its longevity, avoid hard knocks and unduly strong button pressing.
- Extremely cold below 00C, and heat above 1800C may affect the equipment operation in other words, the machine should not operate in extremely cold area or extremely high temperature area.
- Never use volatile fluid such as lacquer, thinner, benzene etc so as to avoid short circuit in the integrated circuit and consequently to prevent insulating breakdown by the fluid.
- No user serviceable part.